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Thin-film transistors fabricated using sputter deposition of zno

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THIN-FILM TRANSISTORS FABRICATED USING SPUTTER DEPOSITION OF ZNO

by

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ABSTRACT

Development of thin film transistors (TFTs) with conventional channel layer materials, such as amorphous silicon (a-Si) and polysilicon (poly-Si), has been extensively investigated. A-Si TFT currently serves the large flat panel industry; however advanced display products are demanding better TFT performance because of the associated low electron mobility of a-Si. This has motivated interest in semiconducting metal oxides, such as Zinc Oxide (ZnO), for TFT backplanes.

This work involves the fabrication and characterization of TFTs using ZnO deposited by sputtering. An overview of the process details and results from recently fabricated TFTs following a full-factorial designed experiment will be presented. Material characterization and analysis of electrical results will be described. The investigated process variables were the gate dielectric and ZnO sputtering process parameters including power density and oxygen partial pressure. Electrical results showed clear differences in treatment combinations, with certain I-V characteristics demonstrating superior performance to preliminary work. A study of device stability will also be discussed.

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CHAPTER 1

INTRODUCTION

1.1 Introduction and Motivation

Silicon-based technologies, such as single crystalline silicon, which have economics of scale, can afford the high-cost materials and complexity of fabrication processes. However the field of large-area electronics, particularly in flat panel display (FPD) area, requires materials which are widely available and economically low-cost. So in the display industry, interest in TFTs that can be fabricated in a cost effective way has become apparent in the past decade [1].

TFTs are used as switching devices for organic light emitting diode (OLED) displays and liquid crystal display (LCD) pixels, as depicted in Figure 1 [2]. TFTs control the amount of light passing through the pixels, which are connected to the addressing lines by TFTs. On one hand, when TFTs are in the on-state, liquid crystal capacitors will be charged which will twist liquid crystals to pass the light through. On the other hand, when TFTs are in the off-state, liquid crystals are disconnected from addressing lines and voltage will be held; static state is preserved. TFTs are now applied in FPDs, from portable devices for GPS, digital cameras and cell phones to large-area format devices for laptops and TVs [3].

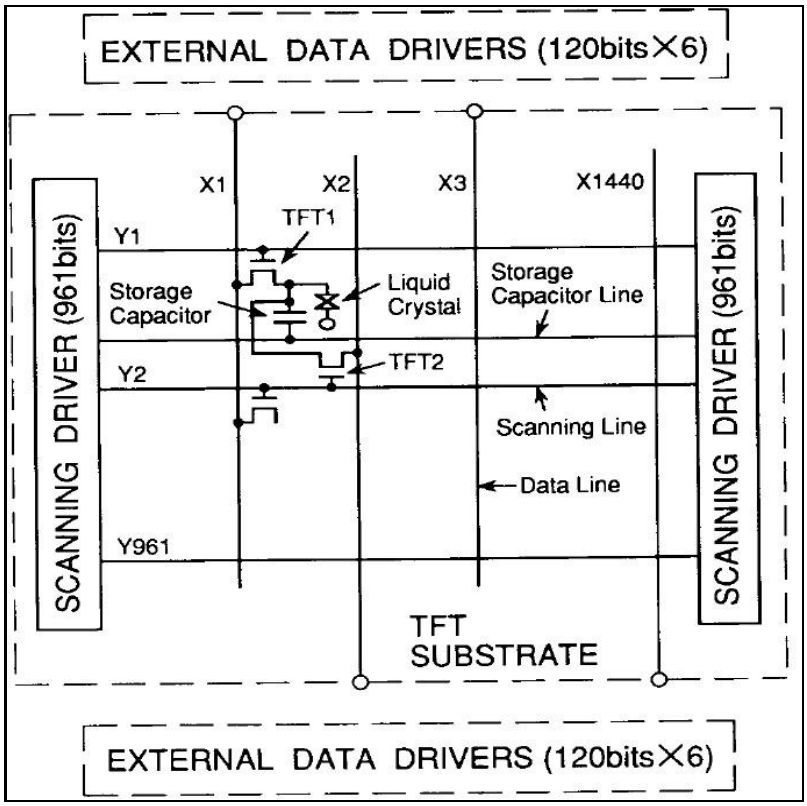


Figure 1: Typical liquid crystal display pixels, TFTs are used as switching devices. [2]

Today, development of the channel layer materials in TFTs has been extensively investigated. This has been due to industrial needs for large-area transparent FPD, in which a-Si, one of the conventional channel layer materials, leads current TFT technology. The performance of a-Si TFTs can easily control the pixels, especially for LCD. However, the low electron mobility and bias stress instability make them difficult to satisfy the performance for image processing in active-matrix OLED (AMOLED) [4]. Another conventional channel layer material: low temperature polycrystalline silicon (LTPS), even though it has higher carrier mobility, the non-uniformity nature of the grain sizes make it undesirable to any of the application in large are electronics.

The push to overcome these limitations continues. Metal-oxide materials that have semiconducting properties, such as ZnO and IGZO, are potential candidates with several advantages in carrier mobility and manufacturing uniformity. In addition, the processes can be carried out at relatively low temperature, and when combined with transparent conducting materials, they can provide high visible transparency [5], [6].

1.2 Work Covered in This Document

The primary focus of this study was to investigate TFTs that are fabricated with sputtered-ZnO as channel layer material. Along with this, a more complete description of metal-oxide semiconductor TFT is given in chapter 2. Preliminary works, sputter system upgrade, process flows and designed experiment will be discussed in chapter 3. Finally, the devices with material characterizations and electrical measurements are shown in chapter 4 and 5. Conclusion and future work will be presented in chapter 6.

CHAPTER 2

CHANNEL LAYER MATERIALS FOR THIN-FILM TRANSISTORS APPLICATION

In the 1960s, the first thin film transistor with a CdS semiconductor as the channel layer material was developed [7]. After 20 years of improvement, the use of silicon-based materials became more pronounced in the mid-1980s, and nowadays a-Si and low temperature polycrystalline silicon (LTPS) TFTs are mature technologies that dominate the FPD arena as switching devices for active matrix liquid crystal display (AMLCD). Metal-oxide semiconductor materials are currently popular areas for research. The benefit of having metal-oxide semiconductors is that they can provide better or at least the same performance for transistors in a smaller geometry, which results in displays with higher pixel aperture ratios and more integration. In this chapter, different materials for current technologies and future research will be briefly reviewed.

2.1 Hydrogenated Amorphous Silicon (a-Si:H)

Over the past two decades, hydrogenated amorphous silicon (a-Si:H) has been a suitable channel layer material in the development of TFTs due to the superb uniformity and low temperature process [8]. It had been known that high quality a-Si:H thin films could be achieved by chemical vapor deposition (CVD) on large area substrates at low cost, particular by plasma enhanced chemical vapor deposition (PECVD). In addition,

silicon dangling bonds can be passivated by hydrogen atoms to form Si-H bonds, which improves the performance of a-Si films [9].

TFTs fabricated of a-Si:H are very attractive to companies because of their low power consumption, due to low leakage, and low cost in large size displays with high production throughput. Typically, the devices have inverted-staggered bottom-gate structures. Figure 2 shows the cross sectional view of this structure. First the bottom-gate electrode, using metals such as chromium or molybdenum, is deposited by sputter deposition. After patterning using photolithography, the gate dielectric layer, such as amorphous silicon nitride (a-SiN_x:H) or silicon dioxide, is deposited via PECVD. Then silicon is deposited at low temperature (T < 550 ℃) in the same chamber. For contact areas, before source and drain (S/D) metal deposition, a thin layer (*i.e.* 500 Å) of phosphorus (P) doped (n^+) a-Si:H is deposited to form ohmic contacts to S/D electrodes. Finally, an overetch is used to remove the n^+ a-Si:H thin layer in the back channel region [9-11].

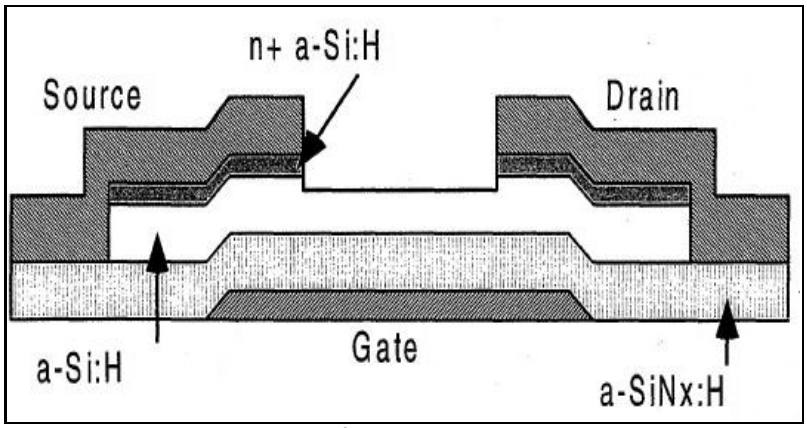


Figure 2: A schematic of typical bottom gate a-Si:H TFT [6].

Recent advances in a-Si:H TFTs have been reported by several research groups. In general, high quality films can be deposited at low rate, which unfortunately reduces the production throughput because of the long deposition time. One solution is to deposit

a-SiN_x:H and a-Si:H layers by multiple steps with different deposition rates. A low rate for the films near the a-SiN_x:H/a-Si:H interface achieves a high quality channel for electron conduction, and a high rate near the gate metal helps to suppress gate leakage. A fast rate can be used for the back channel as well, since it is removed [11]. The other solution is to change the shape of the TFT structure. For instance, Lee *et al.* reported alternatively shaped a-Si:H TFTs to reduce gate source capacitance and leakage current which are important for the application of AMLCD [12].

Although a-Si:H TFTs have been developed over the years and became more efficient for the application of AMLCD with adequate on-state current, yet they continue to suffer from low drain current for a given gate bias due to the low electron mobility (< 1cm^2/V-sec) [8-12], which becomes critical for switching devices in AMOLED. Furthermore, another issue is the instability of a-Si:H TFTs. Since a-SiN_x:H deposited by PECVD has a high level of defects, therefore charge trapping during bias-temperature-stress (BTS) results in a significant threshold voltage (V_T) shift demonstrating electrical instability [13], which potentially leads to image burn-in or image sticking in AMOLED.

2.2 Low Temperature Polycrystalline Silicon (LTPS)

The relatively low electron mobility of a-Si:H TFTs requires external integrated circuits for driving displays like AMOLED. However, with improved performance of poly-Si TFTs, which demonstrate high electron and hole mobility, the integration of the display driver circuits could be accomplished [4]. For fabrication, poly-Si TFTs are achieved by either a top-gate design, which is very similar to that of conventional MOSFET devices, or bottom-gate configurations, which are similar to the a-Si:H TFT design in Figure 2.

The deposition and crystallization processes of poly-Si are critical for performance improvement, which is strongly influenced by grain boundaries and defects in the thin film. In general, a polysilicon film can be deposited by CVD at 580 ℃, but the grain size is typically less than 0.5μm, which will suppress the carrier mobility of TFTs. Therefore, several crystallization methods can be performed to increase the grain size.

First of all, to reduce grain boundaries in the channel layer, solid phase crystallization (SPC) could be done at less than 600 ℃ in nitrogen ambient for tens of hours. Grain size could be enlarged up to several micrometers, and the carrier mobility has been reported around 60cm^2/V-s for these poly-Si TFTs [14]. However, SPC requires long time annealing, which makes it undesirable for large-area FPD. Excimer laser annealing (ELA) is an alternative to SPC and is widely used for crystallization of amorphous silicon. The mechanism of ELA is that silicon is absorbing in the laser output radiation wavelengths, and could be melted without substrate heating [15]. The carrier mobility for ELA that has been reported can be as high as 331cm^2/V-s with the grain size exceeding 4 μm [16]. However, the ELA system suffers from a high cost and narrow process window, so the throughput may not be as good as the SPC. Another crystallization method, metal induced lateral crystallization (MILC) has been reported with carrier mobility above 400cm^2/V-s [17], [18]. Nickel is used as a metal source because of the fact that nickel silicide ($NiSi_2$) has almost the same lattice constants as silicon with less than 0.4% mismatch. After nickel deposition, UV-ozone cleaning is used to induce nickel-silicide nucleation, and then the film is annealed at low temperature for long grains first (*i.e.* ~450 ℃). Once MILC is achieved, the second annealing is performed at high temperature, which will enlarge the width of the grains, finally enhancing the mobility [19].

Even though more stable current can be supplied by poly-Si TFTs for AMOLED than a-Si:H TFTs due to higher carrier mobility, the non-uniformity of grain sizes, which is caused by grain boundary numbers and locations, prevents application in large area displays. Even for small areas, compensation circuits are needed for a uniform image quality [20].

2.3 Metal-oxide Semiconductor Technologies

Metal-oxide semiconductors that are attracting interest today can be divided into two categories: one is polycrystalline metal-oxide semiconductor (*i.e.* ZnO), and the other is amorphous metal-oxide semiconductor (*i.e.* a-IGZO). Both of them can realize transparent electronics due to their large band gap and wide controllability over carrier concentrations.

2.3.1 Zinc Oxide

Zinc oxide is one of the most widely used polycrystalline oxide semiconductors because of the abundance of Zinc-based minerals on earth and its low cost. The band gap has been reported around 3.37eV [21]. Zinc oxide has a wurtzite hexagonal structure that can be described as a number of alternating planes composed of O^{2-} and Zn^{2+} ions with preferred grain growth in the direction of the c-axis [22]. Figure 3 shows the wurtzite structure of ZnO; the gray (small) and yellow (large) spheres denote oxygen and zinc atoms, respectively.

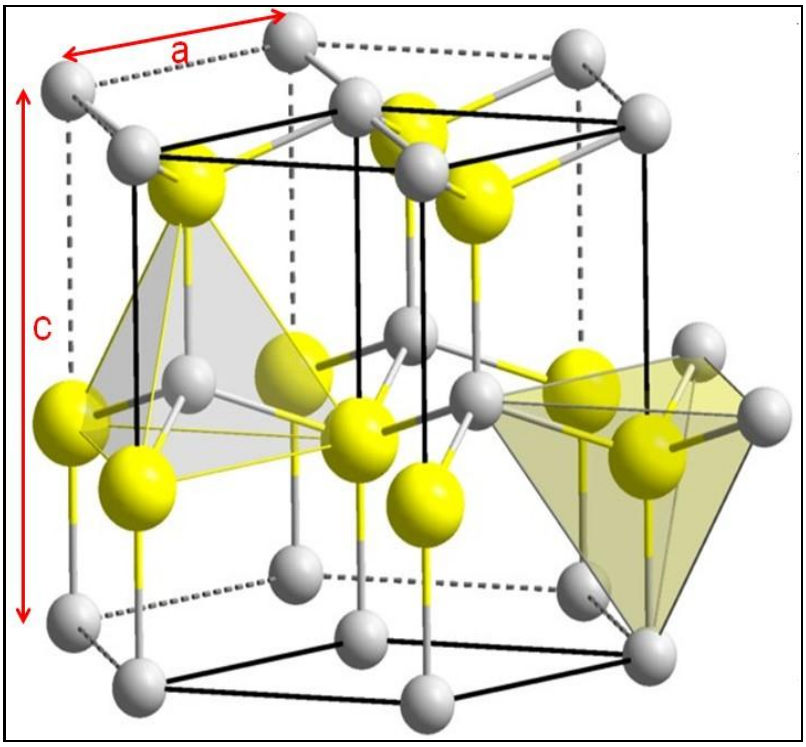


Figure 3: Hexagonal wurtzite structure of ZnO with lattice parameters a = 3.24Å and c = 5.21Å. [3]

Although the free electron concentration in ZnO thin film varies from $10^{13}/cm^3$ to $10^{19}/cm^3$, as deposited ZnO is typically an n-type semiconductor [23]; the conductivity mechanism is still open to debate. Originally zinc interstitials and oxygen vacancies were thought to render ZnO n-type behavior. However recently Van de Walle suggest that hydrogen, which is hard to get rid of during ZnO thin film deposition and common to the fabrication environments, may contribute to n-type conductivity as an electron donor [24]. For p-type conductivity, some groups have reported that by substituting either group-I elements (Na and K) for zinc sites or group-V elements (N, P, Sb and As) for oxygen sites, the n-type doping can be compensated to achieve p-type properties [25, 26]. However this p-type behavior was unstable and the results are questionable since reproducibility was not demonstrated, as reported by Ozgur *et al.* [27].

With semiconducting properties, ZnO has been introduced as channel layer material in TFTs. There are several techniques for ZnO deposition, such as sputtering, molecular beam epitaxy (MBE), pulsed laser deposition (PLD), CVD and atomic layer deposition (ALD). Among these, sputtering and ALD are most popular for ZnO thin films.

Sputtering, including DC and RF sputtering, has been widely used in ZnO TFTs due to its low cost and low operating temperature. Zinc oxide thin films can be obtained by sputtering from high-purity ZnO or metallic Zinc targets. The deposition is carried out in an ambient with Ar/O_2 at a pressure of 1-10mTorr. Oxygen and argon serve as the reactive and sputtering gases, respectively. Oxygen partial pressure plays a vital role in the resistivity of as-deposited ZnO films, as well as the electrical property of ZnO TFTs [28]. Moreover, the distance between target and substrate along with DC or RF power supply can regulate the sputtering yield rate. Hoffman *et al.* fabricated the first n-channel enhancement mode transparent ZnO TFTs with an on/off ratio of 10^7 and electron mobility of 2.5 $cm^2/V\text{-}s$. Since that time the ZnO TFTs have proven their use as switching devices in pixels of AMLCD [23].

Sputter deposited ZnO TFTs have been widely investigated, but few have been reported with high performance. ALD has the advantage of depositing a uniform and conformal film, which proved to be an advanced thin film deposition technique, and has been utilized for ZnO TFTs. During the deposition, two precursors are used; diethylzinc (DEZ) and water, serve as metal precursor and oxidizer, respectively. Inert gas, such as nitrogen, could be used for purging, as well as carrier gas. Reactive gases cycle through the chamber sequentially, and react with a surface chemical to form one atomic layer thin film at a time. The pump and purge time can be adjusted with desired film thickness [29].

The main disadvantage of ZnO by ALD is the high carrier concentration; compensation dopants are needed if enhancement mode TFTs are desirable. Lim *et al* claimed that nitrogen would suppress the high carrier concentration down to $10^{13}/cm^3$ by using 29% NH_4OH [30]. Another method has been studied by Mourey *et al*, who used plasma enhanced ALD (PEALD) for ZnO channel layer deposition. Enhancement mode devices with excellent electrical properties have been reported: mobility was extracted by $16cm^2/V\text{-}s$, on/off ratio > 10^9, subthreshold swing of 0.14V/decade and threshold voltage of 6V [31]. Although the conventional ALD system has several advantages that can produce high quality thin films, another major disadvantage of ALD, in general, is the much slower deposition rate than the other thin film deposition techniques. As an alternative to conventional ALD, a spatial atomic layer deposition (S-ALD) system, developed by Eastman Kodak Company, demonstrates higher deposition rate (> 30Å/s) and potential for low cost commercial use [5].

2.3.2 Indium Gallium Zinc Oxide

Indium gallium zinc oxide (IGZO) is another wide band gap (3.5eV) n-type semiconductor. Crystalline IGZO (c-IGZO) is composed of alternating layers of InO_2 and $GaZnO_4$. Orita *et al.* claimed that overlapping of In 5s orbitals and InO_2 layers form the electronic states at the edge of the conduction band of c-IGZO, and the conduction paths for electrons are served by In 5s states. Moreover, by introducing dopant ions into $GaZnO_4$ layers, high conductivity is achievable [32]. Figure 4 shows the ionic bond structure of c-IGZO. Nomura *et al.* studied coordination structures of amorphous IGZO (a-IGZO) by using extended x-ray absorption fine structure analysis and *ab initio* calculations. It turned out that a-IGZO has a similar bonding arrangement as c-IGZO [33].

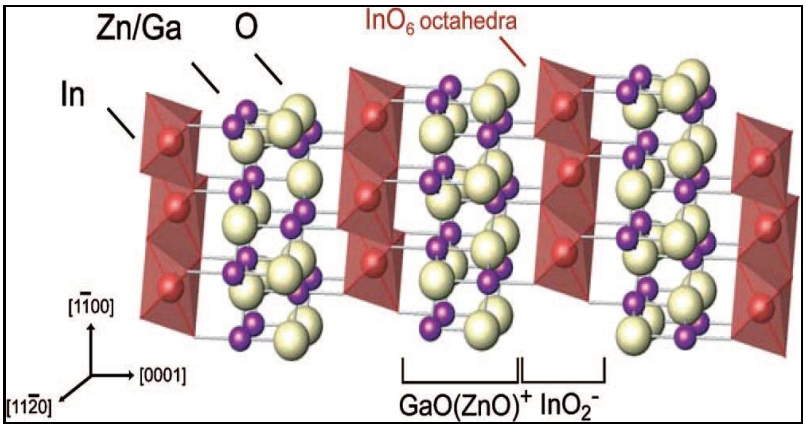


Figure 4: Structure of $InGaZnO_4$ crystal [33]

Because of similar structures between the amorphous and crystalline phase for IGZO material, a-IGZO has been preferred for fabricating TFTs due to its ease of fabrication. Comparing to ZnO, a-IGZO shows superiority in TFT applications because of better control for carrier concentration in the channel layer. It is known that as-deposited sputtered ZnO normally shows high carrier concentration due to the oxygen vacancies created during sputtering, but gallium atoms have stronger bonding to oxygen than zinc or indium atoms. Therefore, they help to suppress the oxygen vacancies and carrier concentration [34]. The electron mobility of a-IGZO has been reported to be more than $10cm^2/V\text{-}s$, which is 10X higher than that of a-Si [6], [35], [36]. The most common methods that have been used for depositing a-IGZO in TFTs are PLD and sputtering.

Suresh *et al* fabricated a-IGZO TFTs with n-channel enhancement mode devices by PLD. TFTs had inverted-staggered bottom-gate structures (similar to that in Figure 2). The deposition conditions were modified by adjusting the oxygen partial pressure and the number of pulses to give required carrier concentration and film thickness. For IGZO thin films, a conductivity of 10^{-3} to $10Scm^{-1}$ can be achieved by varying oxygen partial

pressure. Also the conductivity dropped as a result of increasing the annealing time. Mobility was extracted by 11-15 cm^2/V-s, on/off ratio > 10^7, subthreshold swing of 0.2-0.25 V/decade and threshold voltages of 1-2 V [36].

Jeong *et al.* investigated a-IGZO TFTs by sputtering. An additional SiO_x etch stop layer served as the passivation layer and was deposited to protect the back channels in TFTs. Electrical parameters were extracted: mobility of 17 cm^2/V-s, on/off ratio of 10^9, subthreshold swing of 0.28V/decade and threshold voltages of 1.1V [6]. Fung *et al.* fabricated a similar structure for a-IGZO TFTs by sputtering. Slight differences in electrical parameters were obtained as compared to those by Jeong [35]. Moreover, Yabuta *et al.* built top gate a-IGZO TFTs, in which the conductivity of the film was able to be controlled from 10^{-3} to 10^{-6} S cm^{-1} by mixing oxygen into argon sputter gas [37].

2.3.3 Summary of Metal-oxide Semiconductor TFTs

With superior electrical properties, much better than a-Si, these metal-oxide semiconductors have been proved suitable for large-area AMOLED. To ensure these robust products, electrical stability was evaluated by long-term current temperature stress (CTS) and bias temperature stress (BTS). In both cases, the study has shown that metal-oxide TFT has a smaller threshold voltage shift ΔV_{th} than that of a-Si TFT [13], [35]. All the above properties make these metal-oxide semiconductor TFTs the most ideal choices for a future large area (*i.e.* 82 inch) ultra-definition display [38].

A summary of the key electrical measurements between a-Si TFTs and metal-oxide semiconductor TFTs are presented in Table 1; the data indicates the current best-known results. It is obvious to see that for mobility, metal-oxide semiconductor TFTs have much larger values than those of a-Si TFTs, supporting the application of metal-oxide

semiconductor TFTs for switching devices of large area electronics in image processing of AMOLED.

Table 1: Summarized electrical results of TFTs

	a-Si TFT	*ZnO TFT (Sputter)*	*ZnO TFT (ALD)*	*IGZO TFT (PLD)*	*IGZO TFT (Sputter)*
Mobility (cm^2/Vs)	0.6~0.8 [12]	2.5~10 [23]	15~20 [5, 31]	11~15 [36]	15~20 [6]
Current on/off Ratio	10^7 [12]	10^7~10^8 [23]	10^8~10^9 [5, 31]	10^7~10^8 [36]	10^9 [6]
Threshold Voltage (V)	2.0 [12]	10~20 [23]	5~10 [5, 31]	1.0~2.0 [36]	1.0~2.0 [6]
Subthreshold Swing (V/d)	0.3~0.4 [12]	1.5~2.0 [23]	0.1~0.3 [5, 31]	0.2~0.3 [36]	0.2~0.3 [6]

CHAPTER 3

ZNO THIN FILM TRANSISTOR FABRICATION

3.1 Preliminary Work

3.1.1 Sputtering System

Sputtering is a physical vapor deposition (PVD) process that is common for thin films and widely used in this research work. For DC sputtering the targets must be conductive to sustain the glow discharge. The system is designed with a pair of parallel metal electrodes. A cathode or target is connected to a negative DC power supply; facing the cathode is the anode or substrate, which is usually grounded. The atmosphere is evacuated to high vacuum first. A DC field is applied across the two electrodes, and a glow discharge is maintained by introducing an inert gas, such as argon. With the created plasma, argon ions accelerate to the target, striking the metal atoms. Target atoms will be ejected for deposition, and the liberated secondary electrons sustain the plasma.

In the RIT Semiconductor & Microsystems Fabrication Laboratory (SMFL), both DC and RF sputter systems are available. For this research work, a Nano-master NSC 2000 sputter coater has been used. The system is a programmable logic controller (PLC) controlled table top sputtering system with rotating platen, and has a bell jar chamber that is pumped down to 10^{-6} torr pressure within 10 minutes by a turbomolecular pump. Up to three planar magnetrons are available for sputtering on wafers up to 4 inch diameter. Also, the distance between target and substrate is adjustable for desired deposition rate or uniformity. Two 3 inch targets are installed in the system; one is zinc oxide, and the other

is aluminum. Figure 5 (a), (b) and (c) show the sputter system, targets and system in operation.

(a) (b) (c)

Figure 5: (a). Nano-master NSC 2000 sputter. (b). Zinc oxide target (left) with 99.9% purity made by Kurt J. Lesker company and aluminum target (right). (c). System in ZnO sputtering.

3.1.2 ZnO Thin Film

In this study, ZnO thin film was deposited by the NSC 2000 DC sputter system on a glass slide substrate at room temperature with a ZnO target. The glass slides were cleaned by isopropyl alcohol (IPA) and argon was used as a glow discharge gas. DC power supply was set up for 70W, 75sccm argon was used to achieve a working pressure of 5mTorr and the platen was rotating. The distance between substrate and target were set to as 3, 6 and 12 cm. Pre-sputtering was performed by shielding the shutter for 600 seconds to remove surface contaminants and discharge conditioning of the sputtering target. Sputtering was performed in all samples for 3600 seconds. The crystalline structures of

the films were characterized by X-ray diffraction (XRD) and optical transmission was measured in visible wavelengths by a Perkin-Elmer UV/VIS spectrophotometer. Figure 6 shows the XRD result for the film deposited under the conditions shown in Table 2.

Table 2: Working parameters for ZnO thin film deposited on glass slides substrate

ZnO thin film deposited on glass slides substrate	
Power	70W
Gas Flow	75sccm argon (no oxygen)
Deposition Pressure	5mTorr
Rotating Platen	On
Pre-sputter/Sputter Time	600/3600 seconds
Target Distance	12cm

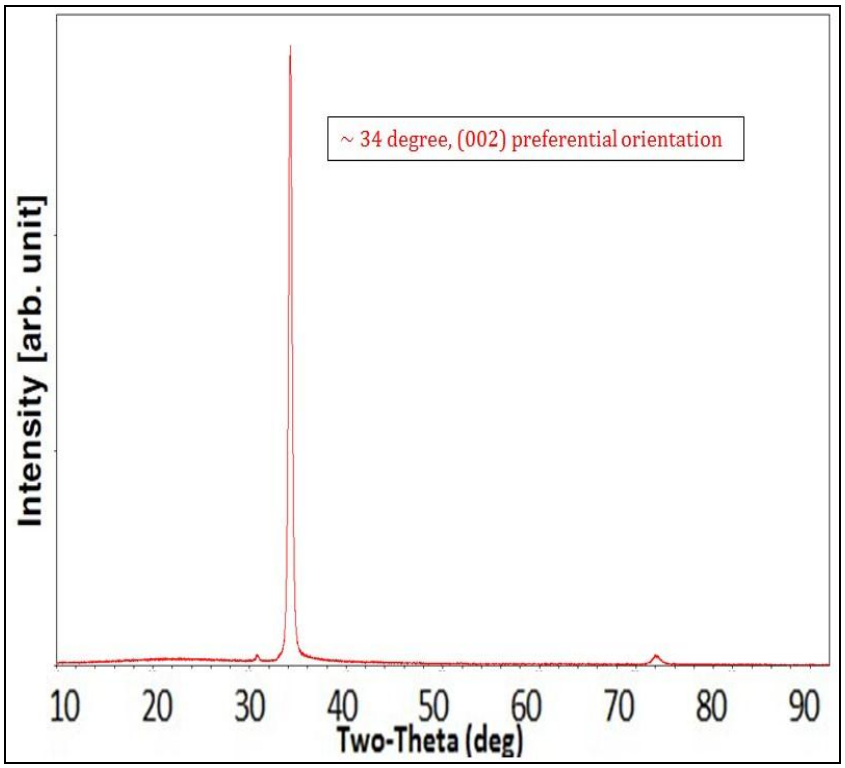


Figure 6: XRD result for the film deposited at 70W, 5mTorr and 12cm separation between substrate and target. Achieved 34° along the 2θ x-axis peak indicates a polycrystalline material with preferred c-axis orientation

XRD was used to analyze ZnO thin film's degree of crystallinity, which is an important parameter describing the structure of the film. As known from the literature, sputtered ZnO thin films always show polycrystalline structure with the c-axis of individual aligned-grains oriented normal to the underlying film, no matter what deposition conditions or substrate types are used. Data was collected from glass slides with ZnO thin film in the XRD measurement. In Figure 6, a clear peak around 34 ° along the 2θ x-axis indicates a (002) plane within polycrystalline material with preferred c-axis orientation [39].

Another material property for ZnO thin film is the optical transmittance. Figure 7 shows the transmission measurement in the visible wavelength with a ZnO thin film of

50nm. Although the data around 630 nm wavelengths is below 80%, this behavior can be explained by destructive interference. Moreover, those results match the literature very well [39], with an average transmission of 84% over the 440-800 nm wavelengths range. For sheet resistance measurement, a CDE ResMap was used for different ZnO samples. Sheet resistance results varied from several Ω/□ to 10kΩ/□; results were not reproducible after some time period and the resistivity kept increasing until the program terminated the measurement due to high sheet resistance which was out of range. There are reports of an immeasurable resistivity of thin ZnO films deposited by sputtering with a high partial pressure of oxygen [40]. Experimental results suggest ZnO films absorb atmospheric oxygen, which may explain why the resistivity kept increasing over time.

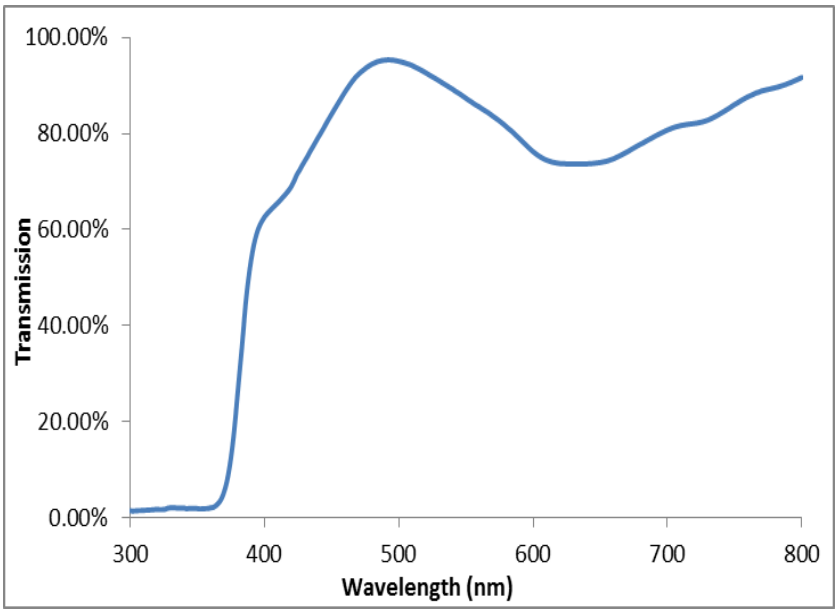


Figure 7: Optical transmission behavior of 50nm ZnO thin film

3.1.3 Initial Study on ZnO Thin Film Transistors

In this research work, a substrate-gate structure was chosen for an initial study on the fundamental electrical properties of ZnO TFTs. Figure 8 shows the main process flow for

ZnO TFT fabrication and top views for different structures that have been made including RingFETs and BoxFETs. The bottom-gate ZnO TFTs start with heavily doped 4" silicon wafers and a 100nm thermal oxide grown at 1000 °C served as the gate dielectric layer. Then 50nm ZnO thin film was deposited by sputtering for 600 seconds, with the settings specified in Table 2. Aluminum was used as S/D electrodes, deposited by flash evaporation and patterned using a lift-off lithography process. A thickness of 100nm was deposited and lift-off was done by ultrasonic with PG-Remover. Figure 9 shows RingFET and BoxFET structures, where the drain is surrounded by the source. These devices are self-isolated and do not require mesa or field isolation for individual device measurement.

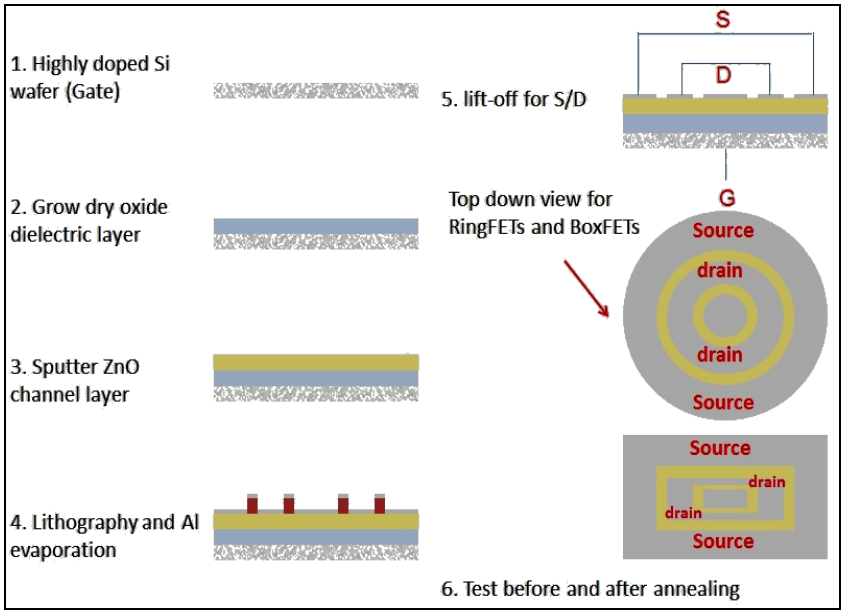


Figure 8: ZnO TFTs fabrication process flow for initial work and top views for RingFETs and BoxFETs structures.

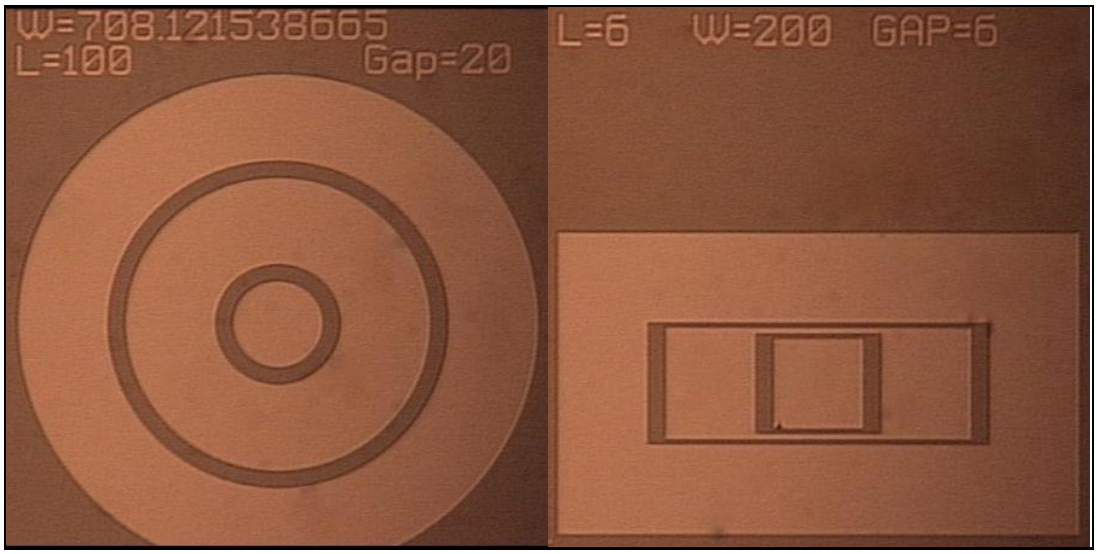


Figure 9: Actual RingFET and BoxFET structures for ZnO TFTs

Electrical properties were investigated in detail in the Microelectronic Engineering test lab using a PC controlled HP 4145 Semiconductor Parameter Analyzer with switching matrix and probe station. Figure 10 shows the family of curves output characteristics of this bottom-gate ZnO TFT under gate to source voltage (V_{GS}) steps ranging from 0 to 40V, and drain voltage (V_{DS}) swept from 0 to 40V during each measurement. A clear saturation region in n-type enhancement mode was obtained, with a positive gate voltage necessary to switching on the transistors. Another important characteristic for TFTs is to evaluate S/D contacts. Non-ohmic contacts will result in nonlinear behavior, which can be observed at low drain bias. The output characteristics in Figure 10 demonstrate ohmic contact behavior where the current-voltage relationship is dominated by the transistor.

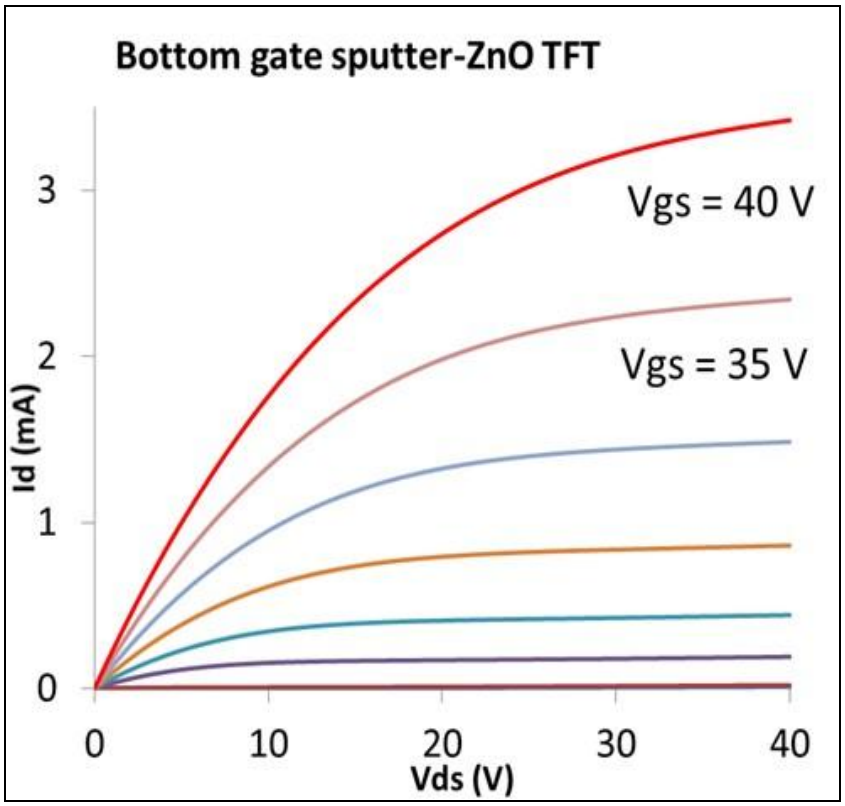


Figure 10: Output characteristics for ZnO TFTs for preliminary work

Figure 11 (a) shows the transfer characteristic on linear and logarithmic scales for linear and saturation regions. Subthreshold swing (SS) was extracted at the maximum slope points on these curves by using the following equation:

$$SS = \left(\frac{\Delta \log(I_D)}{\Delta V_{GS}} \right)^{-1}$$

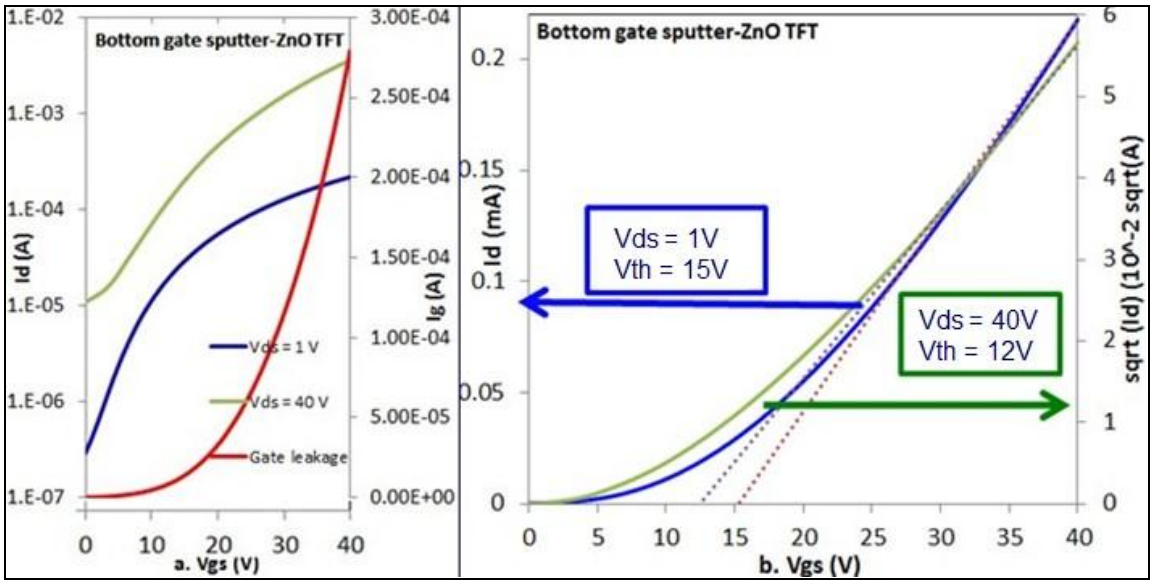
SS values of 5.05 V/decade and 8.89 V/decade were obtained in linear and saturation regions, respectively. These relatively high values may result from the presence of interface traps, which decreases the change in surface potential with gate voltage, and results in poor off-state. This situation may be improved by passivation of interface traps at the interface between the semiconductor channel and the gate dielectric, or decreasing

the gate dielectric layer thickness to achieve a better gate control. Off-state current was also quite high because of the blanket substrate gate, in which case the devices have a large effective gate-source overlap area which is likely to be responsible for high gate leakage current, as seen in 2nd y-axis of Figure 11 (a). The linear scale plots for transfer characteristics are shown in Figure 11 (b) for linear and saturation regions. Threshold voltage (V_{th}) was extracted by standard MOSFET equations in both linear (V_{DS} = 1 V) and saturation regions (V_{DS} = 40 V):

$$I_{DS} = \mu C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)V_{DS}$$

$$(I_{DS})^{1/2} = \left[\mu C_{ox}\left(\frac{W}{2L}\right)\right]^{1/2}(V_{GS} - V_T)$$

where C_{ox} is the gate insulator capacitance per unit area, W and L are the width and length of the TFT, respectively. The straight dash lines in both curves are the best linear fit to the above equations, and the slopes of curves are continuously increasing. Threshold voltage is 15V in linear region, for saturation region, threshold voltage stays at 12V. Finally, Table 3 shows the summary of all the extracted electrical results.



(a) (b)

Figure 11: Transfer characteristics for ZnO TFTs in (a) logarithmic scales for linear and saturation regions (b) linear scales for linear region and saturation regions

Table 3: A summary of extracted electrical results for preliminary work

Extracted electrical measurements for sputter deposition of ZnO TFT		
	Linear	Saturation
Current on/off Ratio	10^3	10^3
Threshold Voltage (V)	15	12
Subthreshold Swing (V/d)	~ 5.05	~ 8.89

3.2 Refinement Towards Improved Device Performance

Based on the results obtained above from the preliminary study, to further develop ZnO TFTs technology, such as lowering the current on/off ratio and subthreshold swing, fabrication process modifications are required.

3.2.1 Nano-master NSC 2000 Sputter System

The sputter system was modified with additional mass flow controllers (MFCs). Three of them were set up as shown in Table 4.

Table 4: MFCs' settings for Nano-master NSC 2000 sputter system

MFCs' Setting	
Gas Flow	*Range (sccm)*
Argon	100
Oxygen	50
Nitrogen	50

3.2.2 Fabrication Process

A modified process was developed; as shown in Figure 12. Starting with highly doped silicon wafers, after RCA clean of all the wafers, a 500nm wet oxide thick film was grown by furnace. Substrate contact holes were patterned and aluminum gate material was sputtered. In this buried gate structure, the silicon substrate still served as a

common gate connection but with smaller effective overlap areas, which should help suppress the high gate leakage that was obtained in the initial study. Next, aluminum was patterned and etched, to prepare for the gate dielectric and channel layer formation. For the gate dielectric layer, PECVD was used to deposit different materials for each treatment combination in a designed experiment.

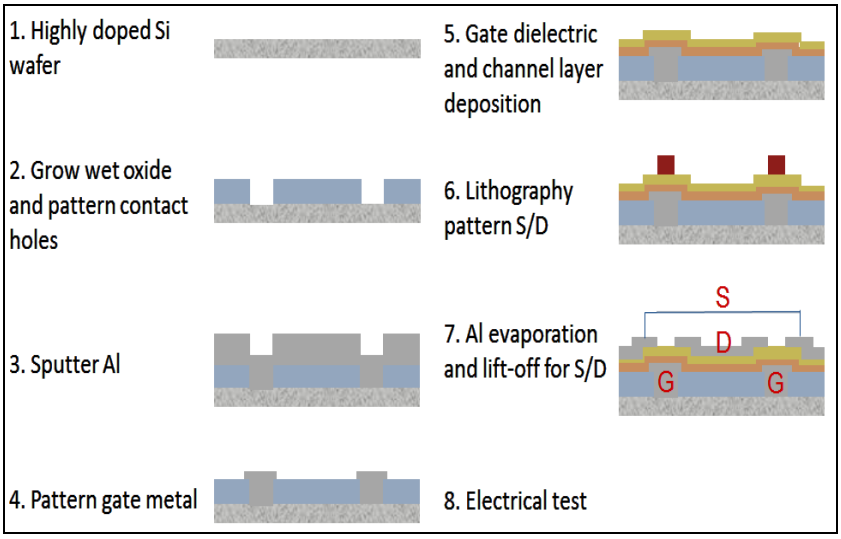


Figure 12: Buried gate fabrication process flow for ZnO TFTs

In order to further investigate ZnO TFTs, an experiment was designed with three variables: different oxygen partial pressure in the gas flows for sputtering, different power density for the sputter system, and different dielectric layer materials. This 2^3 full-factorial experiment required eight device wafers. Another four blank silicon wafers and eight IPA-cleaned glass slides were also included for the purpose of material characterization. Details of the treatment combinations are shown in Table 5.

Table 5: Table of experimental design

Sample (Wafer)	*Sputter Power (W)*	*Oxygen Partial Pressure*	*Dielectric*
1 (N5)	45	10%	100nm SiO_2
2 (N6)	70	10%	100nm SiO_2
3 (N7)	45	30%	100nm SiO_2
4 (N8)	70	30%	100nm SiO_2
5 (P00)	45	10%	SiO_2/SiN_x (15/90nm)
6 (P01)	70	10%	SiO_2/SiN_x (15/90nm)
7 (P02)	45	30%	SiO_2/SiN_x (15/90nm)
8 (P03)	70	30%	SiO_2/SiN_x (15/90nm)

The channel layer ZnO was sputtered by Nano-master NSC 2000 sputter system under the rotation mode. Lift-off lithography with LOR photoresist was performed to pattern S/D regions. After aluminum evaporation and lift-off, the samples were ready for electrical testing.

CHAPTER 4

EXPERIMENTAL DESIGN: MATERIAL PROPERTIES AND ELECTRICAL PERFORMANCE

4.1 Optical Properties and Contact Behavior

For the material characterization, several different types of metrology tools were utilized to collect data, which included variable angle spectroscopic ellipsometer (VASE) for refractive index, SpectraMap for thickness distribution and Perkin-Elmer UV/VIS spectrophotometer for optical transmission. All the results shown here for optical properties and contact behavior characteristics are from sample 4, which had SiO_2 dielectric, 30% oxygen ambient percentage and 70W sputtering power conditions.

4.1.1 Refractive Index & Thickness

Variable angle spectroscopic ellipsometer (VASE) was used to analyze the refractive index of different conditions of ZnO thin films at various wavelengths. During the measurement, a Cauchy model was chosen to fit the measured data, which matched well with literature [27]. Figure 13 shows sample 4 result that refractive index ranged from 1.88 to 2.15 over visible wavelength 400 to 1000nm. With this optical model, Spectramap recipes were created for measuring the ZnO thickness distribution. Thickness data ranged from 20 to 50nm across sample with a mean value of 40nm. While this

inherent variation is significant and in most cases undesirable, it provided a convenient range of thicknesses to assess the influence on device operation within a given sample.

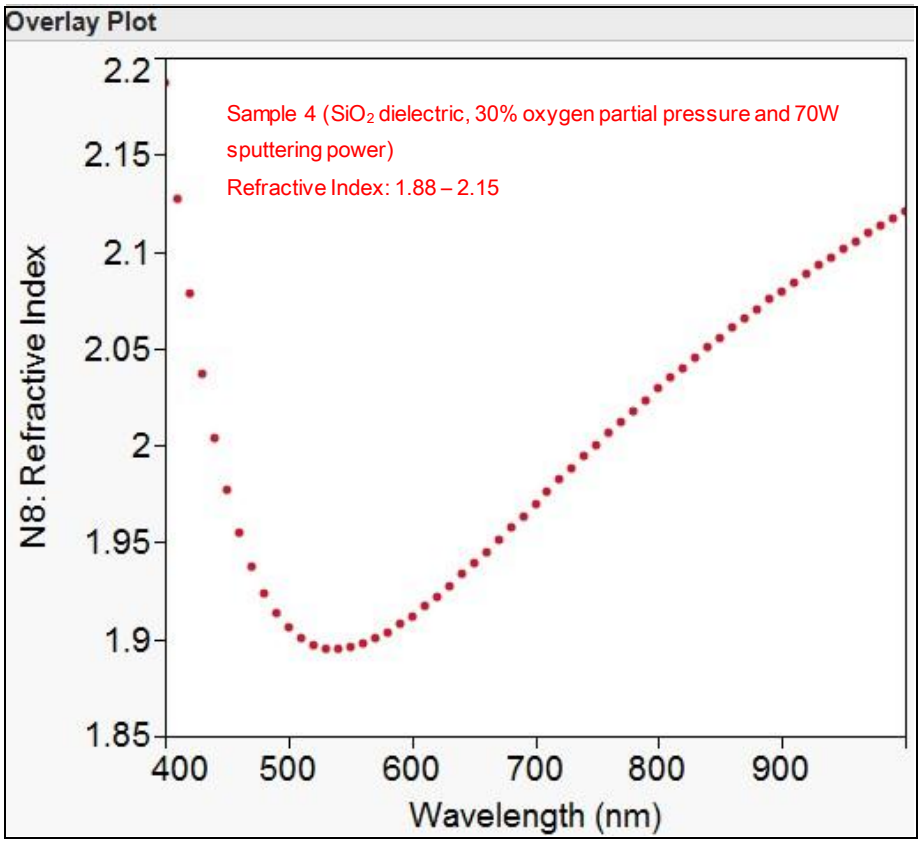


Figure 13: VASE refractive index data of ZnO film at various wavelengths by using Cauchy model

4.1.2 Optical Transmission

Spectrophotometer measurements on glass slides with ZnO thin films were used to determine the optical transmission. The ZnO thin films demonstrated transmittance of 87% over visible wavelengths. The sample 4 data is plotted in Figure 14 with obtained transmittance larger than 90% while the wavelength is above 400nm. Also, it can be seen

that the absorption becomes apparent after 350nm wavelength, and the bandgap energy can be calculated around 3.3eV, which matches the literature [27].

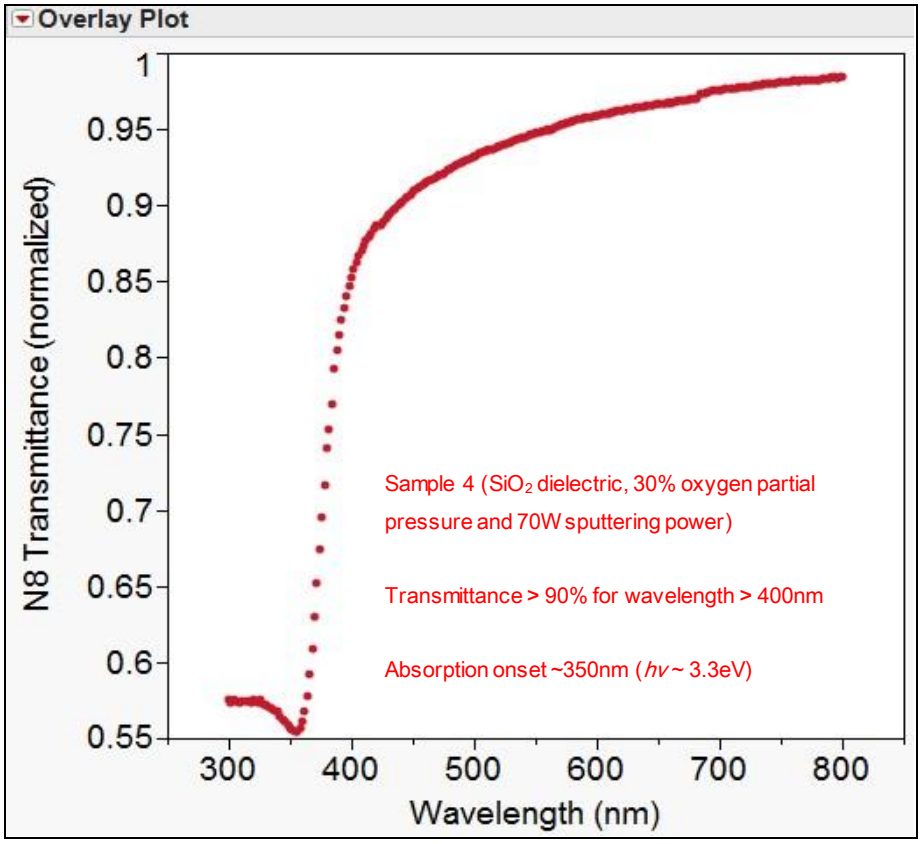


Figure 14: Normalized transmission data of ZnO on glass slides, achieved 90% transmittance over 400nm wavelength

4.1.3 Contact Behavior

Figure 15 and Figure 16 are showing the actual die configuration, common-connection substrate gate boxFET and SEM image of L = 24μm and W = 400μm device, respectively.

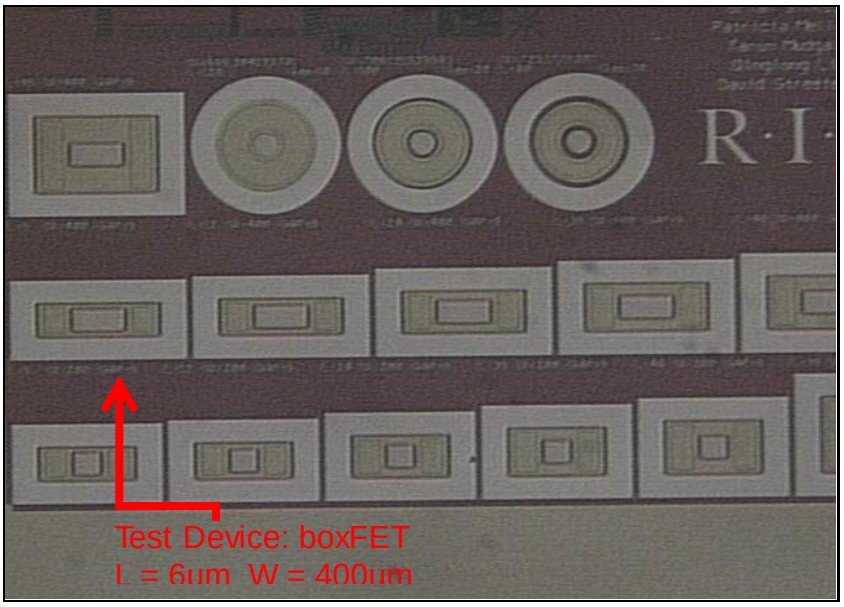


Figure 15: Actual die configuration within a wafer

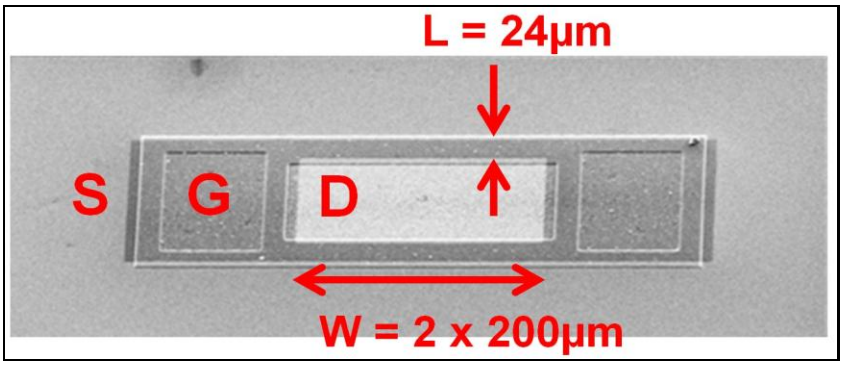


Figure 16: SEM image of ZnO TFT with L = 6µm and W = 400µm testing device

Prior to sintering, there wasn't much current flow through the transistors. I-V characteristics of sample 4 can be seen in Figure 17 and Figure 18 (a). After the sintering in forming gas (5% H_2 in N_2) at 400 ℃ for 30 minutes, most of the devices exhibited transistor characteristics as shown in Figure 18 (b). Sintering establishes ohmic contact

behavior, presumably due to modification of the barrier between aluminum and ZnO. This requires further investigation.

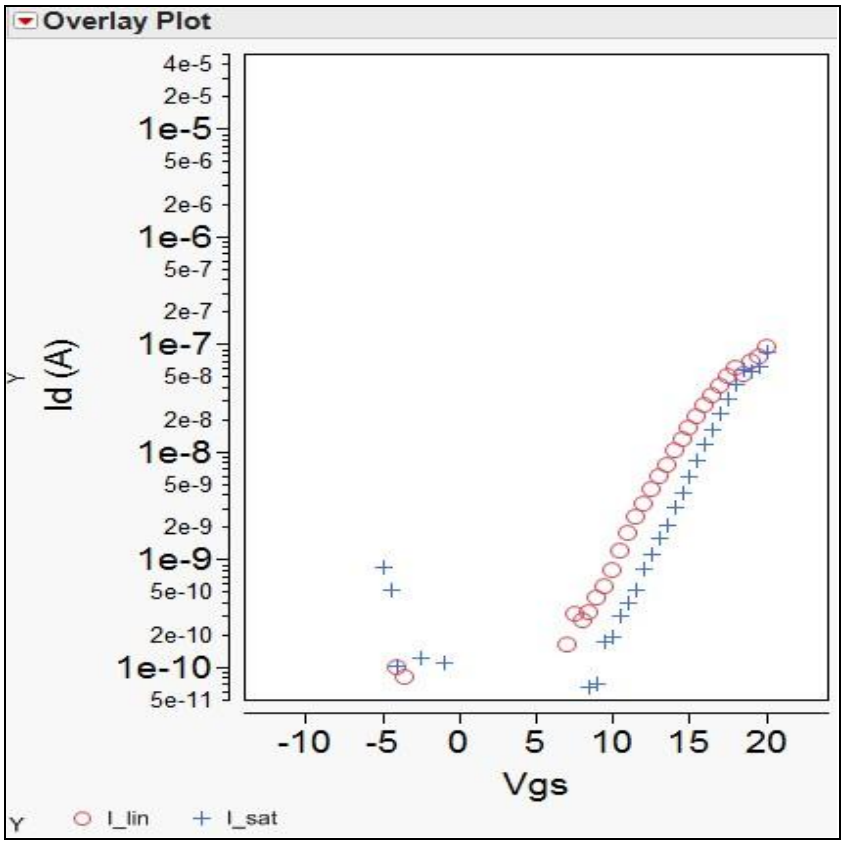


Figure 17: Pre-sintering for I-V curves of sample 4 device with low (1V) and high (20V) drain bias

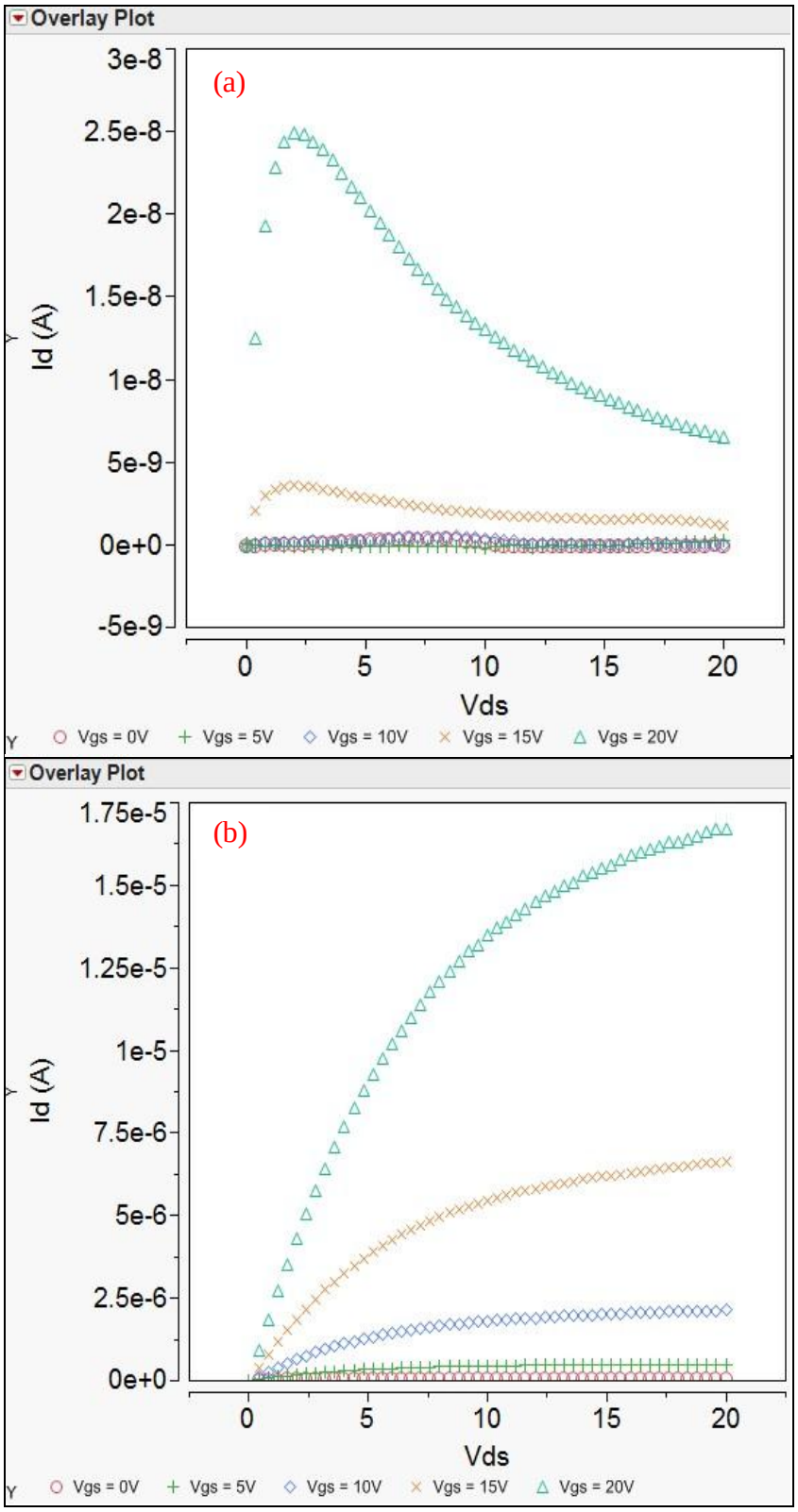


Figure 18: Family of curves on sample 4 device: (a): pre-sintering (b): post-sintering

4.2 DOE Treatment Comparison

The electrical characterization of the fabricated ZnO TFTs was conducted by HP 4145 Semiconductor Parameter Analyzer with switching matrix and probe station. JMP and Microsoft EXCEL software were used to analyze all the data. Device electrical parameters, including threshold voltage, electron mobility, current on/off ratio and subthreshold swing, were extracted and compared. Furthermore, the TFTs were tested again after some time periods to evaluate electrical stability.

4.2.1 ZnO Sputtering Conditions

As seen from Table 5, four sputtering conditions that included sputter power density and oxygen ambient percentage as input variables were employed through the designed experiment. Table 6 shows treatment combinations which had SiO_2 as the gate dielectric.

Table 6: Designed experiment treatments with SiO_2 gate dielectric

Sample (Dielectric)	*Sputter Power (W)*	*oxygen ambient percentage*
1 (SiO_2)	45 (1W/cm^2)	10%
2 (SiO_2)	70 (1.5W/cm^2)	10%
3 (SiO_2)	45 (1W/cm^2)	30%
4 (SiO_2)	70 (1.5W/cm^2)	30%

Figure 19 shows: electrical I-V characteristics for samples 1, 2, 3 and 4, which had SiO_2 gate dielectric. There are several observations that can be concluded from the

measurement results: all of the four samples with oxygen in the sputter ambient, demonstrated improvements in off-state of the devices than the preliminary sputter experiment, which had no oxygen but only argon gas flow, this is presumable due to less oxygen vacancy donor states [41]. Sample 1 demonstrated more depletion mode behavior than the other samples, the devices were already turned on at 0V; sample 2 exhibited kinked subthreshold characteristics; sample 3 had suppressed current at low drain bias, this probably resulted from contact issues (also see family of curves of sample 3 in Figure 20); and finally samples 3 & 4 showed similar off-state behavior with less than 200pA off current. The asterisk shown in sample 4 is because this sample is a best-case treatment for measurement comparisons in this section.

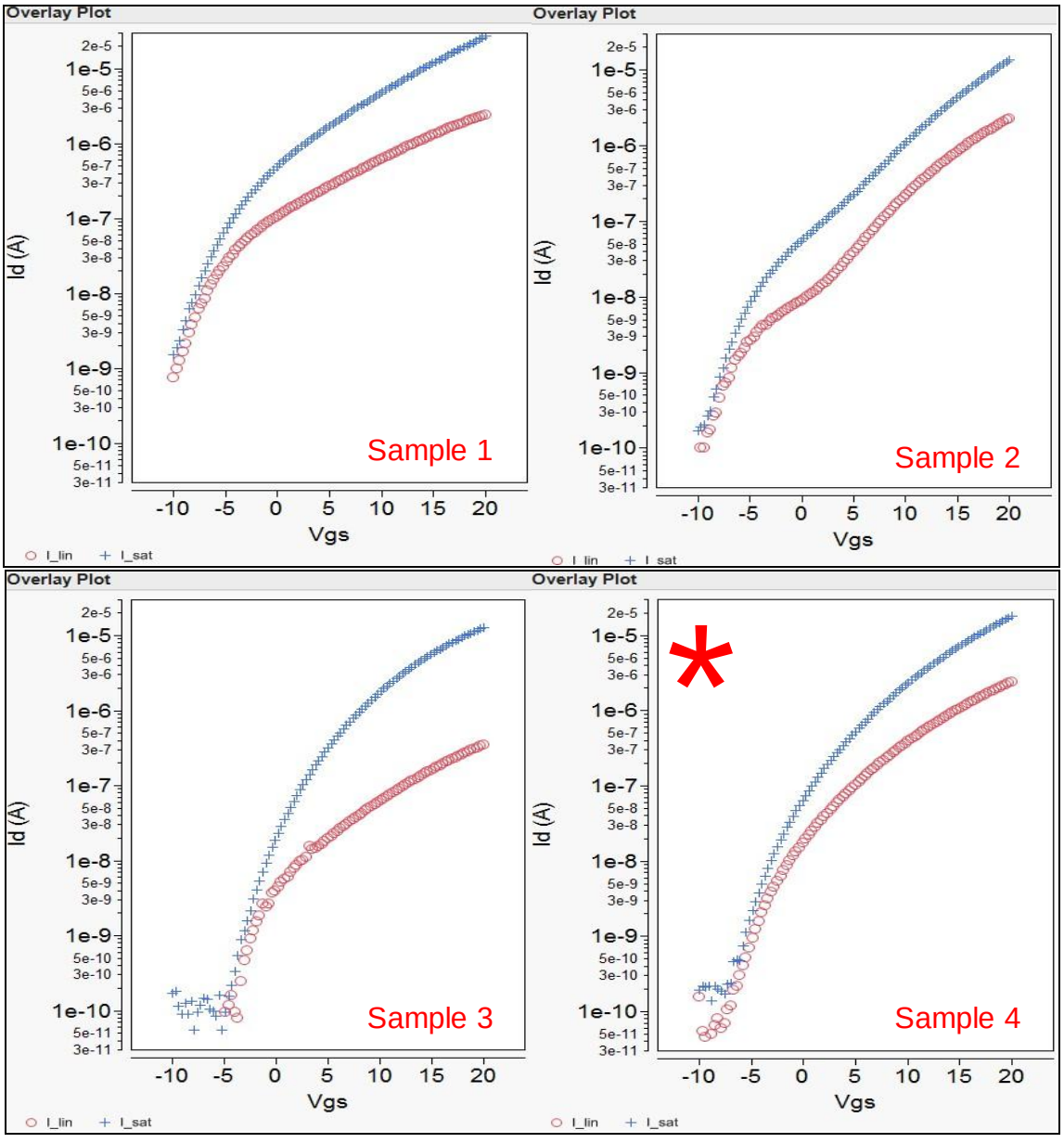


Figure 19: ZnO sputtering conditions: electrical I-V curves for sample 1, 2, 3 and 4 with SiO_2 dielectric

Further investigation was conducted in family of curves for all of the four treatments, as seen in Figure 20 with a consistent y-axis scale. Sample 1 had a negative drain current at high gate bias and low drain bias, which was due to gate-drain leakage. Samples 2 & 3 showed lower drive current; sample 3 indicated non-ohmic contact behavior at low drain bias; and sample 4, as the reference in the experiment, demonstrated the best comprehensive results.

As a summary of the above discussed results for both I-V and family of curves, it seems that sample 4 which had 1.5W/cm^2 sputter power density and 30% oxygen partial pressure sputtering condition was the most satisfactory result. The reasons may be that higher the power, the denser the film, and the lower the density of structural defects with less voids. This probably is the reason why samples 1 & 3 with low power density condition were observed with contact issues (negative drain voltage at 0V), in which more electrons were trapped by those voids. Moreover, the higher power will result in higher rate of sputter gas dissociation and more ionization of the sputtered metal, all of which should contribute with better conformal film properties [42], [43].

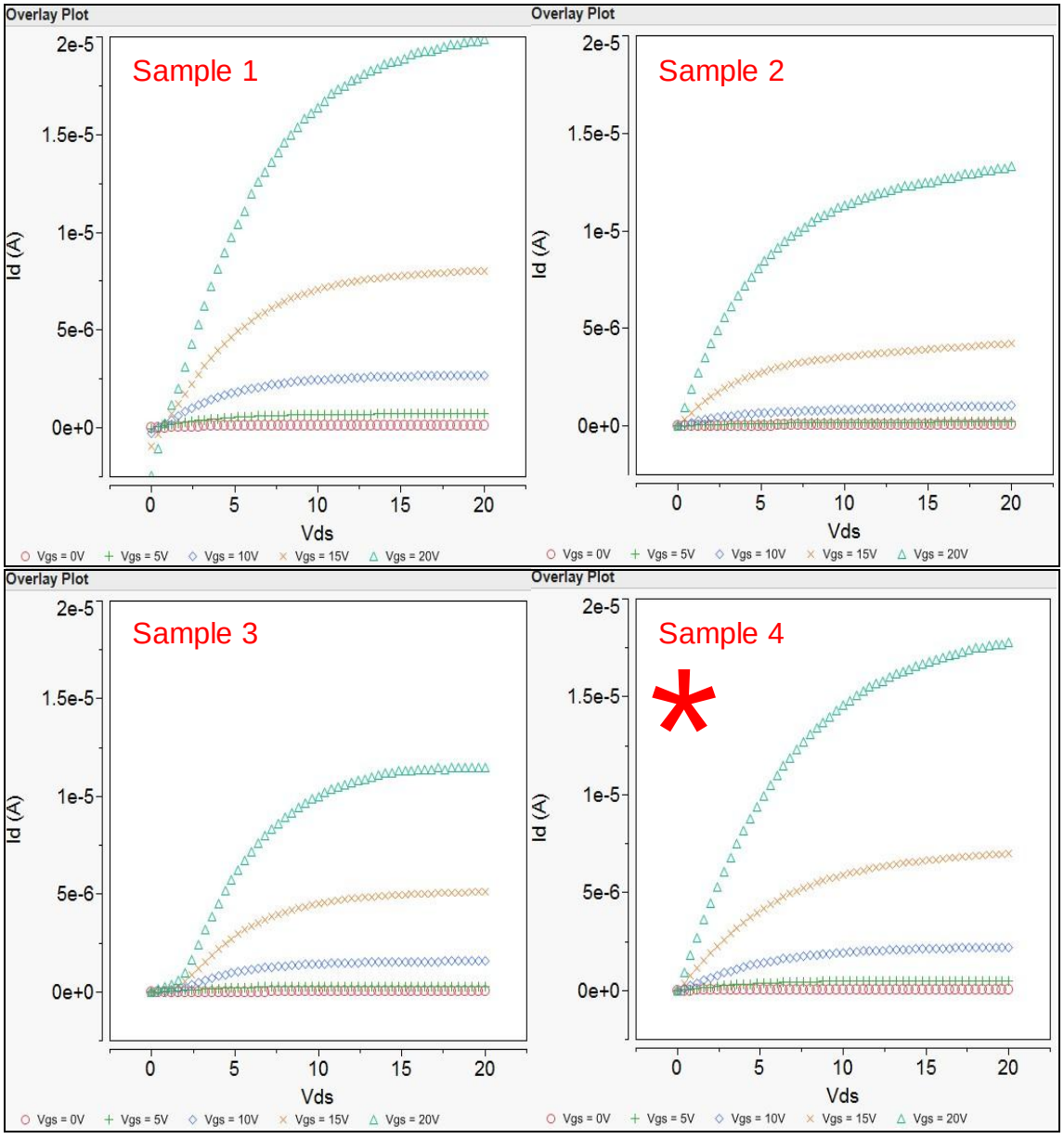


Figure 20: ZnO sputtering conditions: electrical family of curves for sample 1, 2, 3 and 4 with SiO_2 dielectric

The high oxygen partial pressure in the fabrication process also indicated some advantages. In deposited ZnO films, oxygen vacancies that act as shallow donors are one type of the abundant defects, and they can be compensated by oxygen that makes the channel less conductive by reducing free electrons. So with more oxygen introduced, less density of oxygen vacancies are present [41]. Table 7 shows the summary comparison of sputtering conditions.

Table 7: Summary of sputtering conditions

Sputter Conditions		*Sample 1*	*Sample 2*	*Sample 3*	*Sample 4*
Aluminum Contact Ohmicity		Ohmic	Ohmic	Non-ohmic	Ohmic
Gate Leakage (Negative Drain Current)		Pronounced	Not observed	Not observed	Not observed
Transistor Characterization	Drive Current (A)	2e-5	1e-5	1e-5	2e-5
	Off Current (A)	1e-9	1e-10	1e-10	1e-10
	On/Off ratio	2e4	1e5	1e5	2e5
	Subthreshold Swing (V/d)	~ 5	~ 4	~ 2	~ 2

4.2.2 ZnO Layer Thickness

Besides the designed experiment with sputter conditions that had already been discussed, ZnO channel thickness effect was further investigated. Two different devices with ZnO thicknesses of 30nm and 40nm were compared for sample 4. As shown in Figure 21 and Figure 22 in both I-V and family of curves. Minor differences within sample were observed for this ZnO thickness factor, and as expected, the thinner ZnO

layer showed improved off-state, whereas the thicker ZnO layer revealed higher current drive.

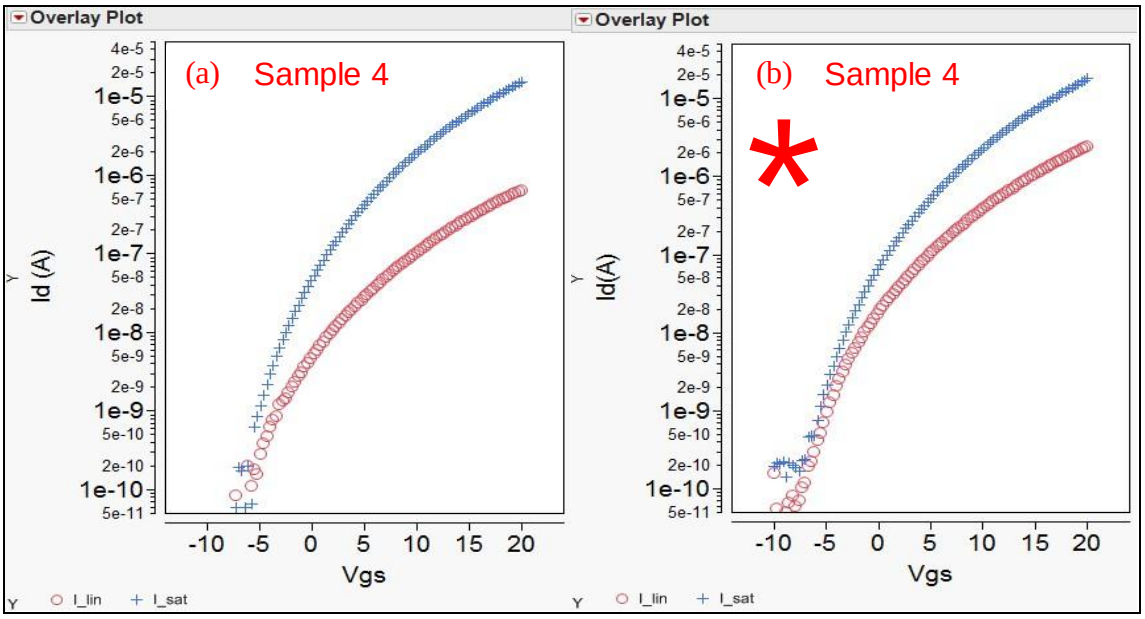


Figure 21: ZnO layer thickness comparison in I-V curves: (a) 30nm (b) 40nm

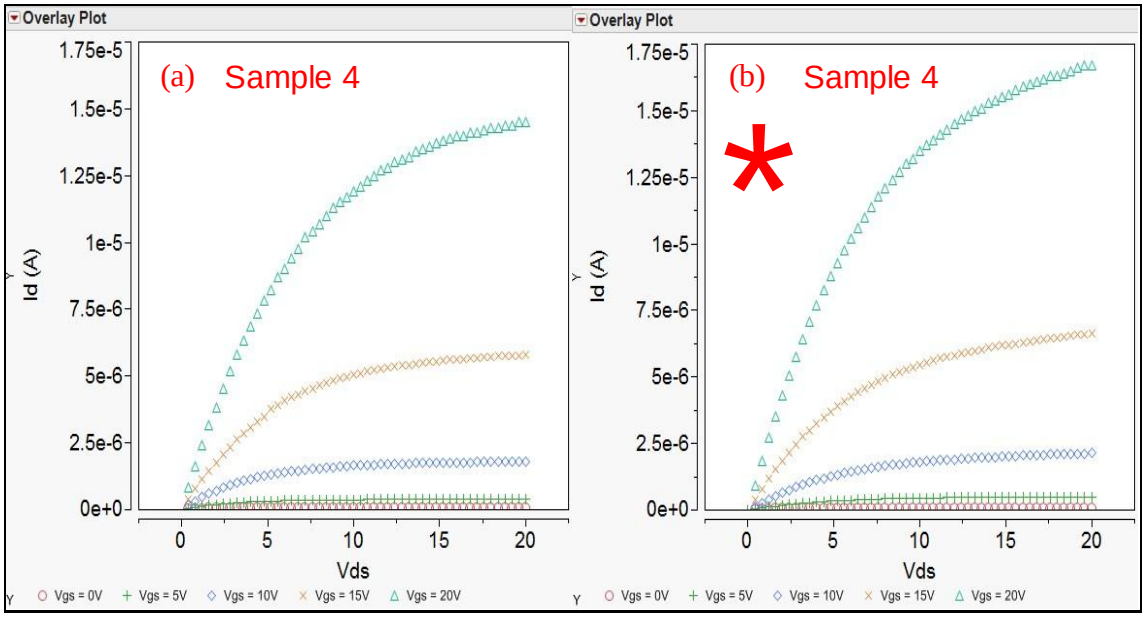


Figure 22: ZnO layer thickness comparison in family of curves: (a) 30nm (b) 40nm

4.2.3 Dielectric Performance

As seen from Table 5, two dielectric materials were studied in the designed experiment, which were 100nm SiO_2 and 15/90nm SiO_2/SiN_x stack. As group 1 with SiO_2 dielectric treatment (samples 1-4) had already been discussed in the previous ZnO sputtering conditions section. Group 2 with SiO_2/SiN_x dielectric (samples 5-8) are now discussed. Some of the group 2 devices were destroyed at the beginning of testing, which means the breakdown voltages were lower than those of SiO_2 only dielectric group 1 devices. So the gate voltage sweep was reduced to -5V to 15V from -10V to 20V for group 2 to avoid further destruction. The low drain bias and high drain bias were set as 1V and 15V, respectively, for both groups during the measurement.

Figure 23 shows measurements on different samples in group 2. All SiO_2/SiN_x dielectric treatment showed distorted characteristics, and it also seems that I-V curves in group 2 were suffering from cross-over effect between the linear and saturation conditions. Further investigation indicated that this phenomenon was not real and actually it was due to hysteresis. For example, a vertical line was drawn at gate voltage of 5V in sample 8, and two data points were extracted at both low and high drain biases. It was noticed that the extracted drain current value at high drain bias was lower than that found at low drain bias. However in Figure 24, which shows the zoomed in picture for the family of curves of sample 8, it can be seen that the curves were well-behaved and did not exhibit negative differential resistance (NDR: lower current at higher drain bias). At the gate voltage of 5 V, the drain current was gradually increased until it hit the saturation region.

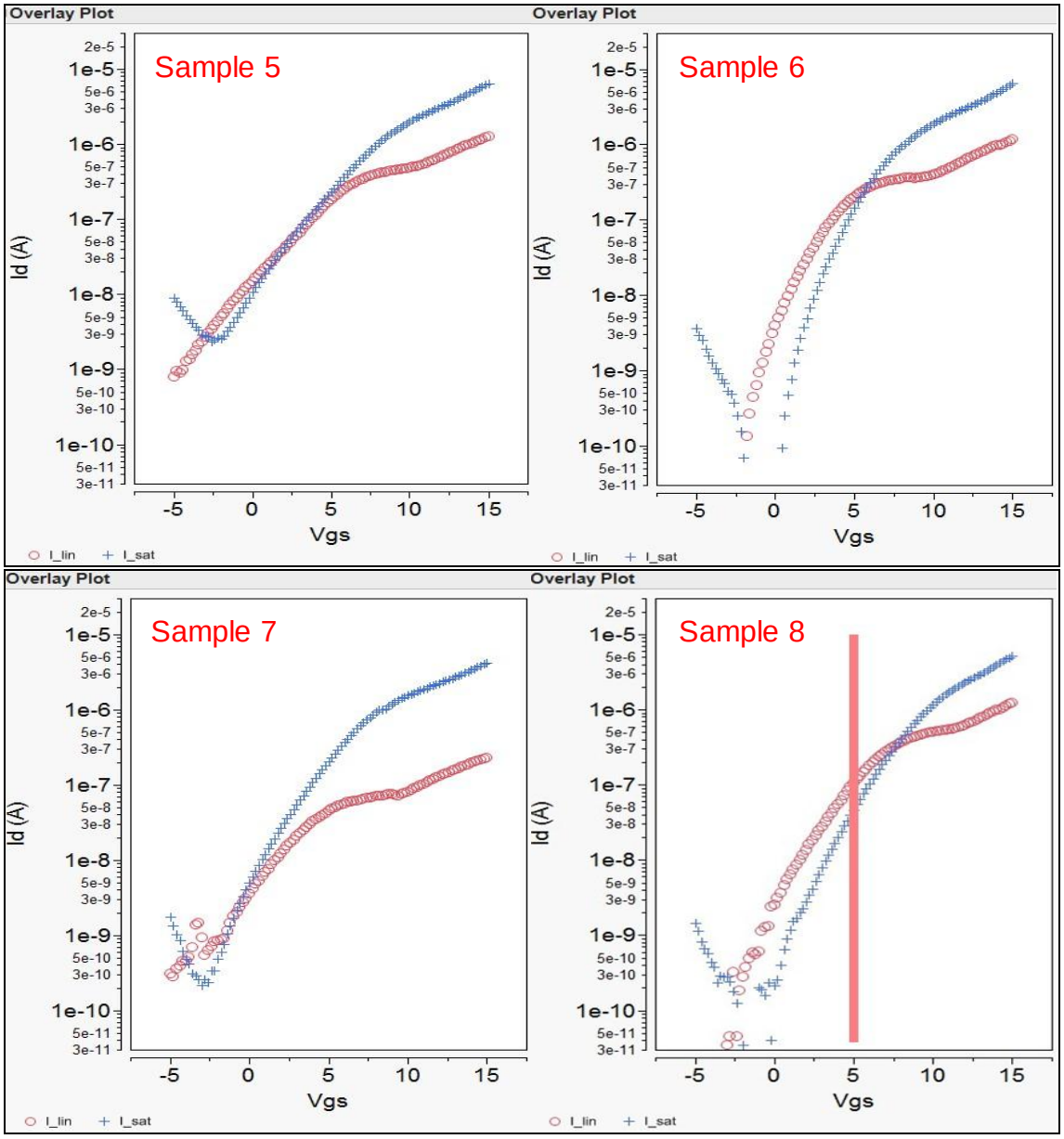


Figure 23: Dielectric performance: electrical I-V curves for sample 5, 6, 7 and 8 with SiO_2/SiN_x dielectric

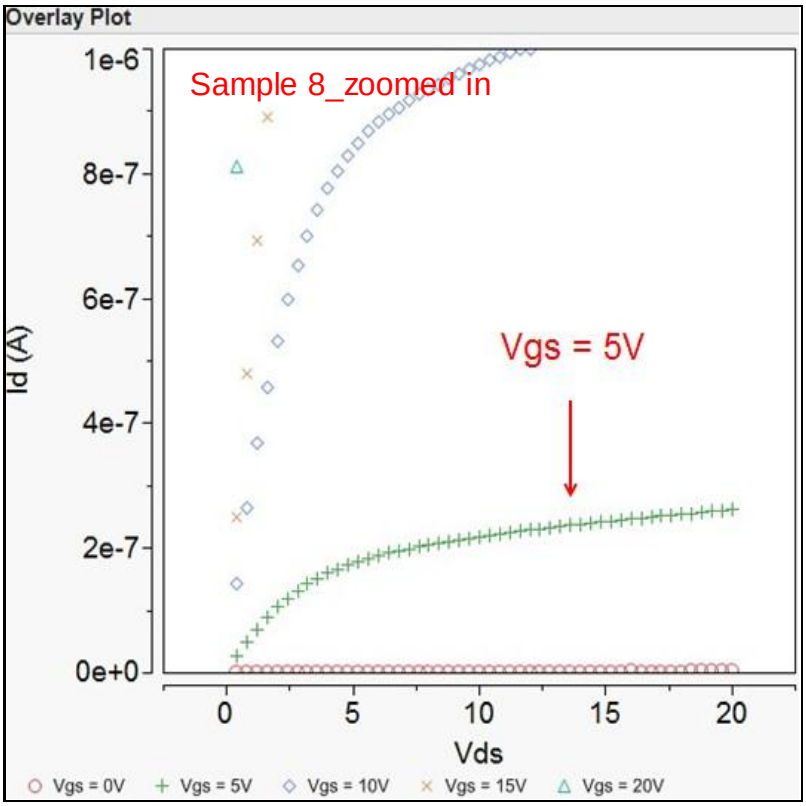


Figure 24: Dielectric performance: electrical zoomed-in family of curves for sample 8 with SiO_2/SiN_x dielectric

The reason for this different observation between the I-V and family of curves can be explained by hysteresis. The order of voltage assignments did matter, which resulted in a different current response. During the I-V test, low drain bia at 1V was applied first to collect linear region data, then after that the drain bia was raised up to 15V for the saturation current measurement. But at the end of the linear region measurement, the gate voltage was also raised as high as of 15 V. This high gate voltage caused traps: either SiN_x/ZnO interface traps or traps into the SiN_x dielectric, which become more negatively charged (or less positively charged) in the ZnO channel, causing a right-stretch in the I-V characteristic taken at low drain bias; then the charges remained long enough in the charged state to appear as a right-shift on the I-V characteristic taken at high drain bias,

as seen in Figure 25. To avoid this, one can increase the number of sweeping steps during the family of curves output measurement. For instance, a hundred steps could be used instead of only 5; the data of drain bias at 1V and 20V can be extracted and plotted separately. Moreover, some negative gate voltage can be applied between the low and high drain bias testing to empty electron traps. All of these methods could help with obtaining I-V measurements without an apparent hysteresis effect. The influence of interface traps is pronounced on group 2 devices.

Gate leakage at negative gate voltage was also explored. At high drain bias, all of the characteristics were exhibiting "GIDL-like" effect, which means the gate overdrove in the off-state on these samples, and could perhaps be gate leakage between gate and drain.

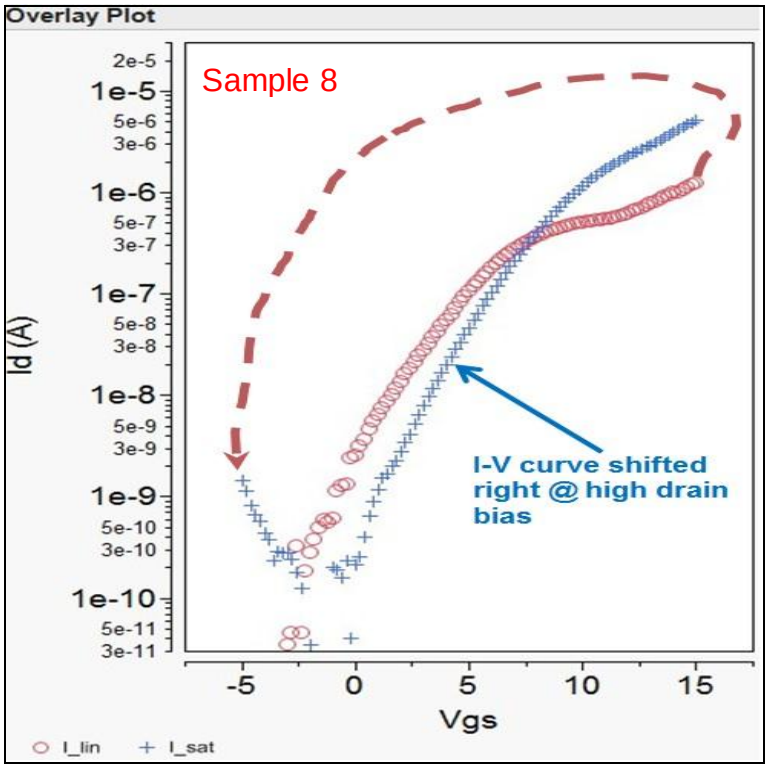


Figure 25: Dielectric performance: electrical right shifted I-V curve at high drain bias for sample 8 with SiO_2/SiN_x dielectric

Table 8 shows the summary comparison between the two different dielectric materials. Based on the data, it can be concluded that SiO_2 dielectric devices have superior performance compared to the SiO_2/SiN_x dielectric devices.

Table 8: Summary of dielectric comparison

Dielectric		SiO_2 (sample 4)	SiO_2/SiN_x (sample 8)
Dielectric Breakdown Voltage		> 20 V	< 20 V
Gate Leakage (Negative Drain Current)		Not observed	Pronounced
Hysteresis (Cross-over Effect)		Not observed	Pronounced
Transistor Characterization	Off Current (A)	1e-10	1e-10
	On/Off ratio	1e5	5e4
	Subthreshold Swing (V/d)	~ 2	~ 2.5

4.2.4 Device Stability

In order to explore the stability of the tested devices, all of the transistors were re-tested after 6 month period. During this time, the devices were stored in air ambient. It turned out that the devices with SiO_2/SiN_x dielectric were more stable than those of the SiO_2 dielectric ones. Figure 26 presents I-V curves of sample 6 at a high drain bias, one of the SiO_2/SiN_x dielectric transistors testing results. From the picture, it can be seen that I-V curves at two different times were comparable in the saturation region.

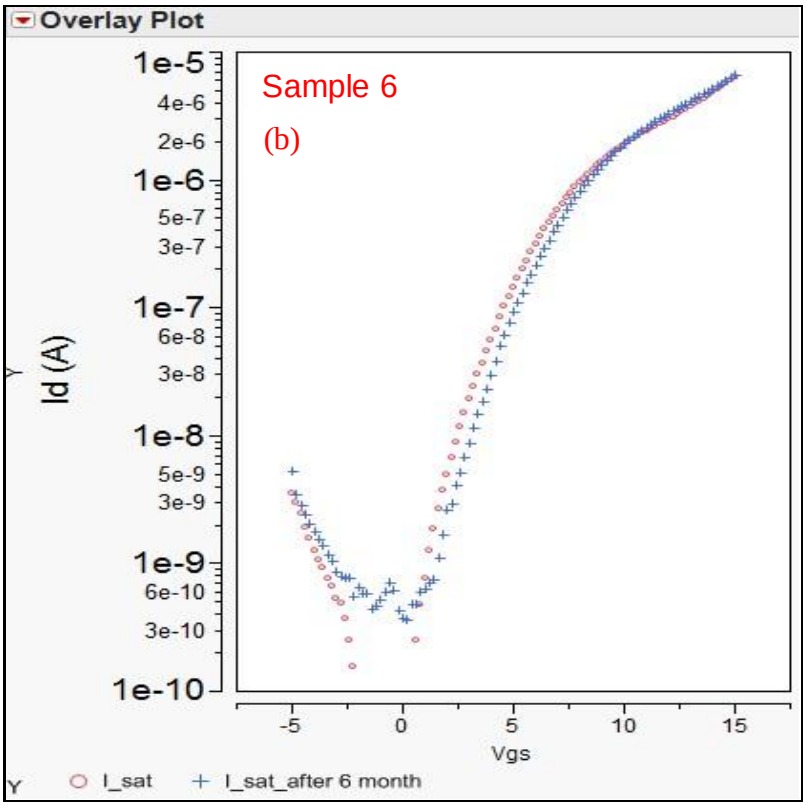


Figure 26: Device stability: electrical I-V curves for sample 6 with SiO_2/SiN_x dielectric: pre and post 6 month measurement at high drain bias

For the SiO_2 dielectric devices, as seen in Figure 27, the I-V curves changed significantly after 6 months. The off current was much higher at high drain bias. The nitride dielectric layer acted as a diffusion barrier preventing loss of oxygen, which helped to suppress the formation of oxygen vacancies within the ZnO film during aging. This is the reason why more leakage and less stable devices were observed with SiO_2 dielectric devices after the 6 month testing. Figure 28 (b), which shows the family of curves after 6 months, further reinforces the above hypothesis, since there was a current flow at zero gate voltage. Even though the drive current was higher after the time frame, it most likely resulted from increased channel conductance due to oxygen vacancies.

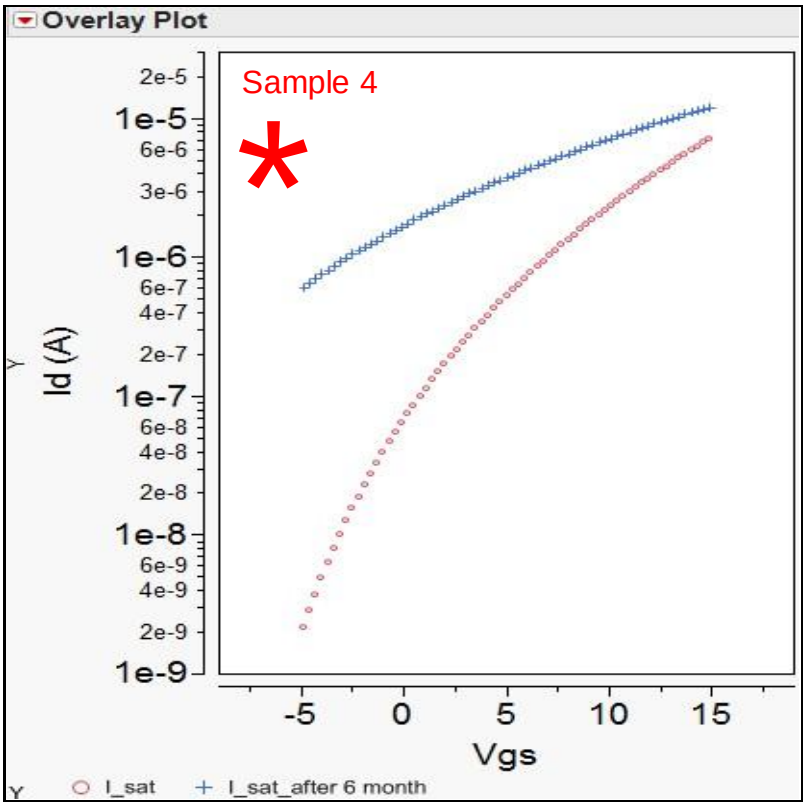
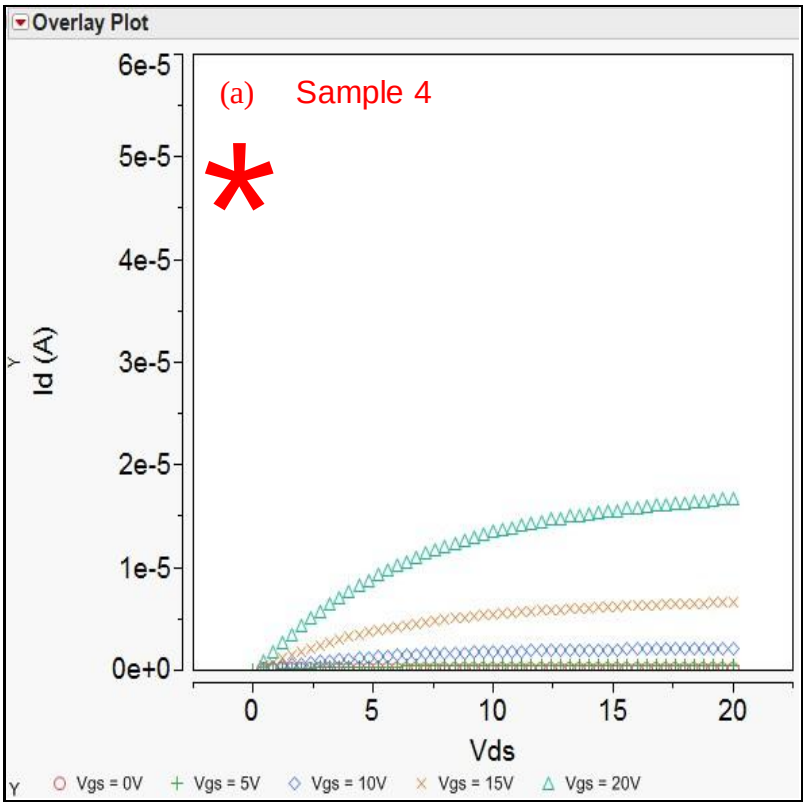


Figure 27: Device stability: electrical I-V curves for sample 4 with SiO_2 dielectric: pre and post 6 month measurement at high drain bias



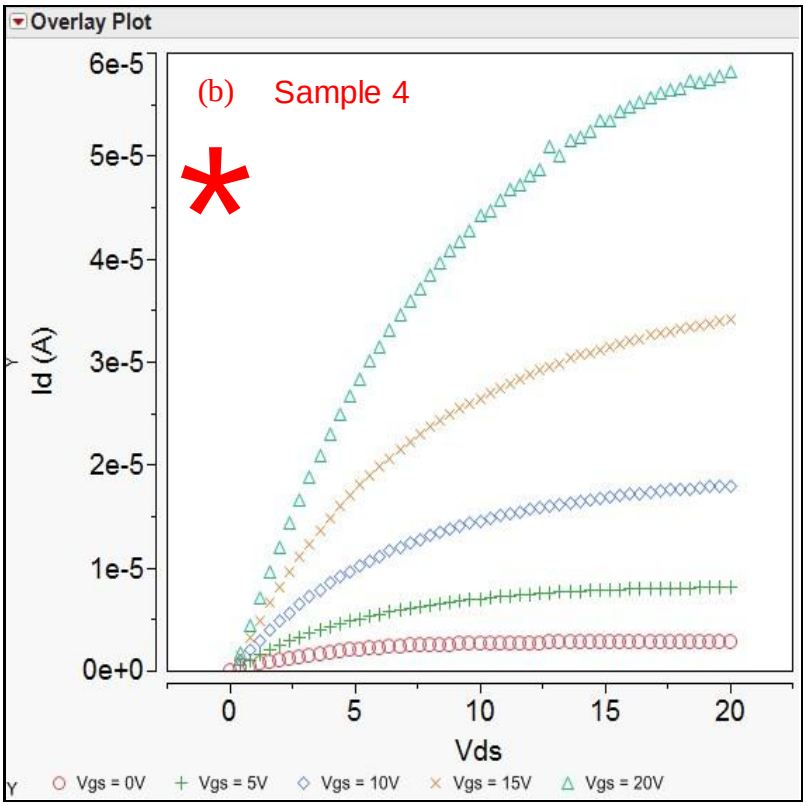


Figure 28: Device stability: electrical family of curves for sample 4 with SiO_2 dielectric (a) pre 6 month measurement (b) post 6 month measurement

Re-sintering was investigated to see if the degradation was reversible. While sintering does not involve an O_2 ambient, hydrogen in the ambient or residual oxygen in the atmospheric furnace, may alter the free electron concentration in ZnO. Exactly the same recipe was applied with forming gas (5% H_2 in N_2) at 400 ℃ for 30 minutes. Unfortunately, the samples were destroyed. During the 6 month open air ambient exposure of wafers, moisture from the atmosphere may have been absorbed, which may have resulted in the destruction of devices during sintering.

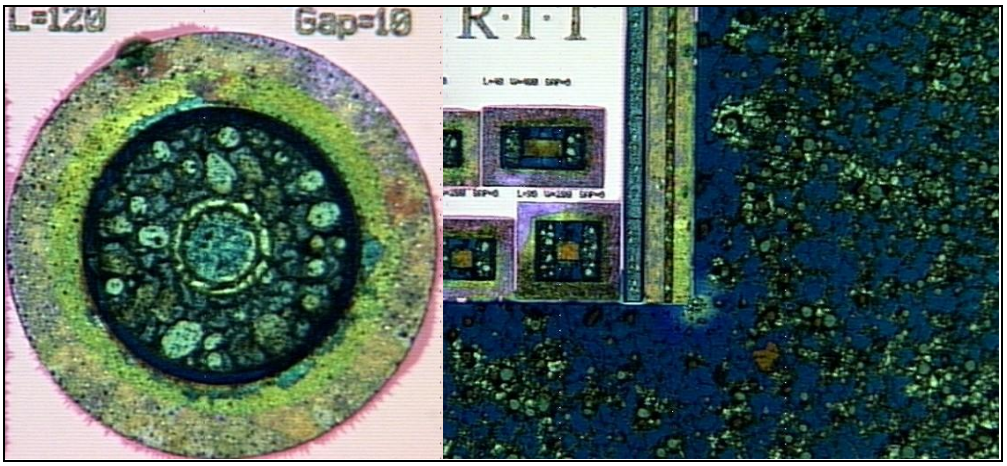


Figure 29: Single device and die images after re-sintering

4.2.5 Summary of Design of Experiment

As a summary of the designed experiment, it seems that the condition for sample 4, which had silicon dioxide dielectric, 30% oxygen ambient, and 1.5W/cm^2 sputtering power density, were more favorable than the other device conditions. Although it showed unstable behavior after some time periods, but it can be solved by improving passivation behavior during the fabrication. The transfer and output curves can be seen in Figure 30.

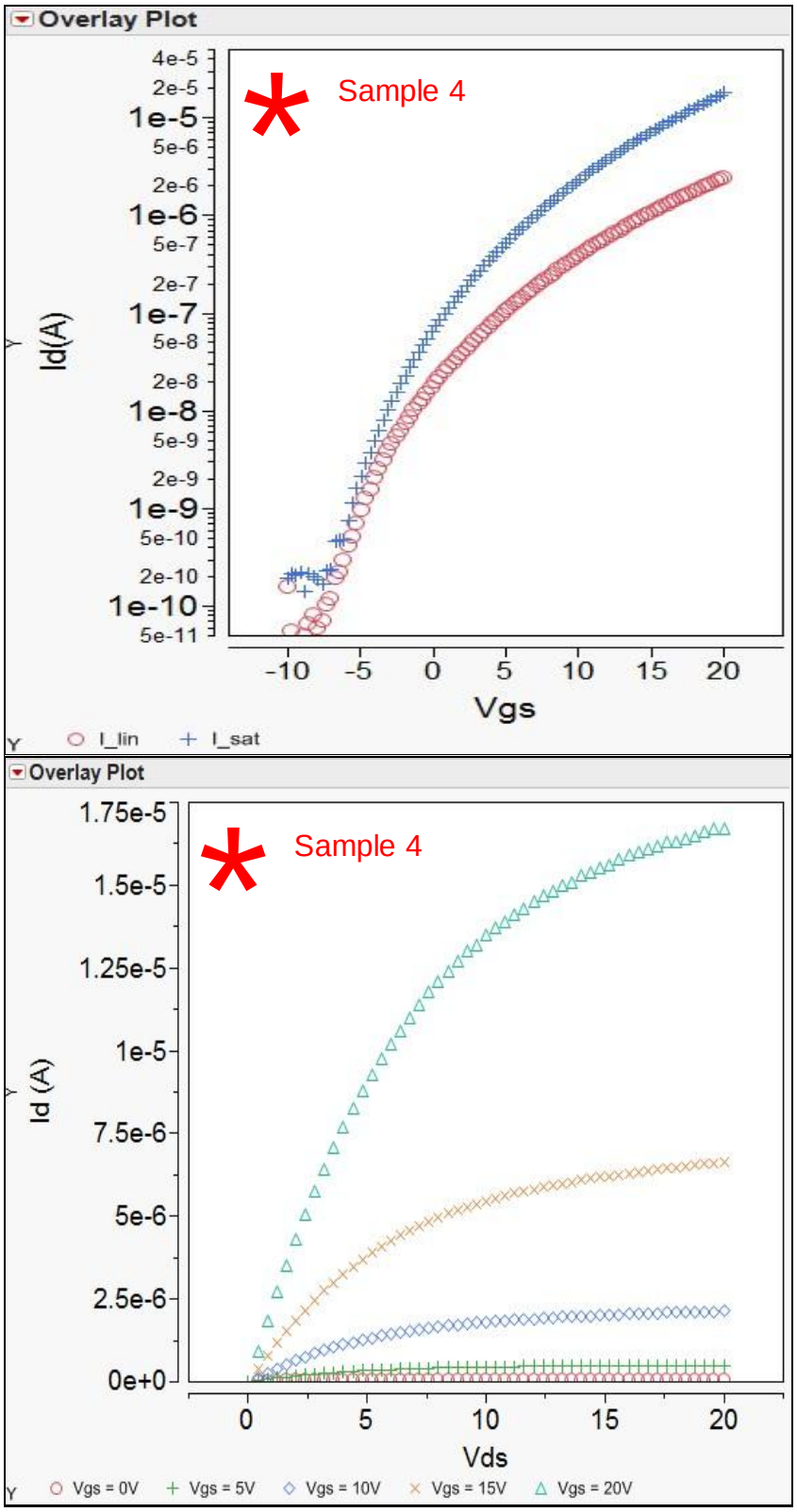


Figure 30: Best comprehensive treatment: Sample 4 with SiO_2 dielectric, 1.5W/cm^2 sputtering power density and 30% of oxygen partial pressure

Electrical parameters were also extracted as shown in Table 9, it shows that on/off current ratio was largely improved to 10^5, and threshold voltage was dropped down to around 5V, subthreshold swing was improved as well, around 2V/d. Mobility was calculated by two methods, one was using utilized standard MOSFET I-V relationships and the other was using transconductance theory. Both of the calculated values are below $1cm^2/V{\cdot}s$. The reasons that these relative small values were achieved can be explained as follows. Figure 30 and Figure 31 demonstrate: (1) continuously changing subthreshold swing; (2) super-quadratic saturation behavior in the family of curves; and (3) ambiguous threshold voltage extrapolation. These characteristics do not follow established off-state and linear & saturation mode relationships, and prevent a meaningful extraction of traditional performance parameters.

Table 9: A comparison of extracted electrical results between preliminary work and designed experiment

Extracted electrical measurements for sputter deposition of ZnO TFT

	Preliminary Work	Designed Experiment (sample 4)
Current on/off Ratio	10^3	10^5
Threshold Voltage (V)	12	5
Subthreshold Swing (V/d)	~ 8.89	~ 2
Electron Mobility ($cm^2/V{\cdot}s$)	NA	< 1

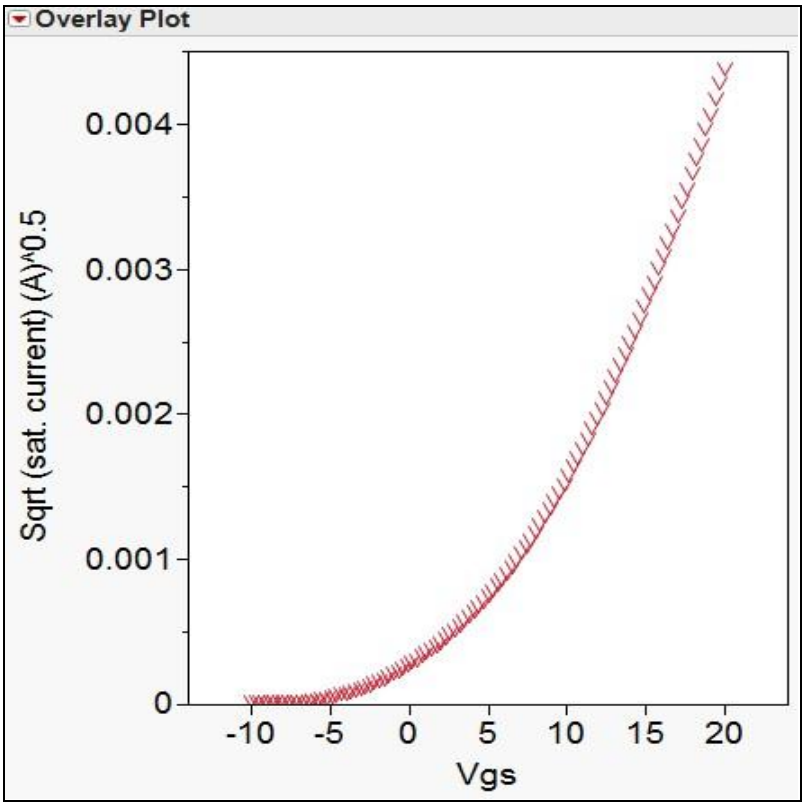


Figure 31: Square root of transfer characteristic for sample 4 for saturation region operation

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 Introduction

TFTs that have application in large area electronics have received considerable attention in the flat panel display area. Interest in ZnO, which is a metal-oxide material that has semiconducting property, is rapidly emerging due to its potential advantages as a channel layer material. In this work the initial realization of TFTs with ZnO as the channel layer led to a detailed investigation. Material characterization and interpretation of TFT characteristics has provided a solid understanding of the physics involved in the metal-oxide material and device system. In this chapter, conclusions throughout the experiment of study will be reviewed and the need for further investigation identified.

5.2 Conclusion of This Work

Throughout this study there were several conclusions reached. In preliminary work, argon-ambient sputtered ZnO thin films were characterized. XRD analysis showed 34 ° peak along the 2θ x-axis, which indicated a polycrystalline film with c-axis preferred orientation. Optical transmittance showed an average of 84% over the visible spectrum. The ZnO TFTs were fabricated with bottom-gate structure under these sputter conditions. Electrical test results exhibited n-type enhancement mode devices with current on/off

ratio of 10^3, threshold voltage of 12V, and subthreshold swing of 8.89V/d at high drain bias. A poor off-state current was attributed to a large effective overlap area between the blanket substrate gate and source. A relative high subthreshold swing was associated with interface traps.

Modifications of the sputter system and process flow were implemented to improve upon the identified weaknesses. The sputter system was modified with additional MFCs to enable sputtering in O_2 ambient. The device structure and fabrication process was modified to restrict the effective gate-source overlap areas which helped suppress the high gate leakage observed in preliminary work. Based on the new tool setup and new revised process, an experiment with 3 input factors was designed, which included ZnO sputtering conditions with different power density, oxygen ambient percentage, and different dielectric material. Optical properties and contact behavior of the modified process were characterized. Sintering with forming gas (5% H_2 in N_2) at 400℃ for 30 minutes was proven to be required to provide ohmic aluminum contacts.

Thin film transistors fabricated within the experimental design resulted in several conclusions. A reference treatment (sample 4) was identified to provide the best comprehensive (on-state & off-state) performance. This treatment had a high-level power density and high-level oxygen ambient percentage, resulting in a high-quality ZnO film [42, 43] with a relatively low free carrier concentration due to suppressed oxygen vacancies [41]. Sample 4 had a SiO_2 gate dielectric, which demonstrated much less evidence of interface traps exhibited by PECVD SiN_x dielectric treatments. Oxide treatments had well-behaved I-V characteristics without significant hysteresis shown on the nitride treatments. Oxide treatments also demonstrated lower gate leakage and higher

breakdown voltage. Some electrical parameters were extracted: current on/off ratio ~10^5, threshold voltage ~ 5V, and subthreshold swing ~ 2V/d. Regarding the electron channel mobility, less than 1cm^2/V·s was obtained. However this relatively low value can be explained by irregularities in the I-V characteristics which prevented a meaningful extraction of certain traditional performance parameters.

Stability testing demonstrated an advantage of the SiN_x gate dielectric. Tested devices were re-tested after 6 month time period stored in air ambient. The SiN_x dielectric revealed a more stable behavior over SiO_2 treatment over 6 month of storage. It appeared that the SiO_2 dielectric did not prevent oxygen outdiffusion from the channel region, resulting in a more conductive (depletion-mode) device with enhanced leakage.

5.3 Future Work

This thesis focused on sputtered ZnO thin film material characterization and TFT device fabrication and test. Certain additional investigations are needed to validate hypotheses and clarify results. Specific areas include sintering for aluminum contact formation, and improvements in ZnO/dielectric interface passivation. Ongoing work on ZnO and IGZO TFTs taking place at RIT will benefit significantly from the research investigations presented in this work.

APPENDIX

Step-by-step process flows for fabricating ZnO TFTs.

Process Flow		
#	**Process**	**Comment**
1	Create Lot Notebook	Important lot processing information sheet
2	Scribe	Use diamond tip scribe on heavily doped wafers
3	Initial Inspection	Use Lecia Microsope to record any defects
4	RCA Clean	Initial clean to remove any defects on the wafer
5	Field Oxide Deposition	Use Bruce furnace tube 1 to deposit 5000A oxide
6	Oxide Thickness Measurement	Use Spectramap to measure field oxide thickness
7	Photo to Pattern Contacts to Substrate	Use GCA stepper with g-line resist to do lithography
8	Oxide Etch	Use Bufferd Oxide Etch (BOE) to remove any native oxide before Al gate deposition
9	Deposit the Gate Metal	Use CVC 601 sputter for Aluminum depostion
10	Photo to Pattern Gate Metal	Use GCA stepper with g-line resist to do lithography
11	Etch Aluminum	Remove Al that not covered with resist
12	Gate Dielectric Deposition	Use P5000 PECVD for SiO2 and Si3N4 deposition (two treatment combinations)
13	Channel Layer Deposition	Use NSC 2000 Nanomaster Sputter for ZnO deposition (treatment combinations include different sputtering power density and different oxygen partial pressure)
14	Photo to pattern S/D	Use GCA stepper with g-line resist to do lithography

15	S/D Formation	Use Flash Evaporator for 1000A Aluminum evaporation
16	Lift-off	Use LOR double layer resist and PG remover to form S/D regions
17	Electrical testing	HP 4145 Semiconductor Parameter Analyzer with switching matrix and probe station
18	sintering	Use Bruce furnace tube 5 with forming gas to sinter fabricated devices
19	Electrical testing	HP 4145 Semiconductor Parameter Analyzer with switching matrix and probe station

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